New Technology-Driven Approaches in the Design of Preamplifiers for Condenser Microphones

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DTU Electrical Engineering
Department of Electrical Engineering

New Technology-Driven Approaches in the Design of Preamplifiers for Condenser Microphones

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Preface

This thesis is submitted in partial fulfillment of the requirements for obtaining the Ph.D. degree at the the Technical University of Denmark, DTU Elektro, Centre for Physical Electronics. The work was carried out from July 2005 to April 2009 including 9-month period of leave. The project has been supported by Pulse MEMS ApS (former Sonion) and the Ministry of Science Technology and Innovation (Ministeriet for Videnskab Teknologi og Udvikling) under the Industrial PhD Programme (http://en.fi.dk/research/industrial-phd-programme). The topic of the thesis is the design of CMOS preamplifiers for condenser microphones. The work on the thesis has been accomplished under the supervision of the company supervisor Lars J. Stenberg, Ph.D. and the university supervisor Prof. Erik Bruun. The thesis was started under supervision of Prof. Pietro Andreani. In the last three months of the project Pirmin Rombach, Ph.D. took over the role as company supervisor, due to a change of job.

Abstract

The topic of this thesis is the design of CMOS preamplifiers for condenser microphones. Increasingly popular type od condenser microphones are MEMS (micro-electro-mechanical) microphones which pose a stringent requirements to the design of the interface electronics among other due to their increased noise. Besides that, as MEMS microphones are easy to integrate with the CMOS circuitry, CMOS circuit design gains importance because it can contribute to the overall improved performance of the system by introducing extra functionalities.

Possible methods of sensing a signal from the microphone are investigated and explained in this thesis. The method resulting in the overall best performance has been chosen for implementation.

Due to the fact that the electronics noise performance is an important factor for minimization of the overall noise of the system, with $1/f$ noise dominant at low frequencies and increasing with CMOS technology shrinking, the investigation of $1/f$ noise in CMOS has been done and is explained along with measurement results in the second part of the thesis. In the third part, the knowledge about the transistor noise previously obtained has been applied to a problem of noise optimization of a CMOS interface for a capacitive sensor.

Finally, in the fourth part, a novel preamplifier designed demonstrating a concept of differential operation of two microphones biased with voltages of opposite polarities has been described. The amplifier shows how accompanying electronic circuitry can be used to enhance performance of MEMS microphones. A new enhanced performance microphone chip-scale package (CSP) with two microphone dies and the CMOS amplifier has been assembled being the microphone with several dB higher signal-to-noise-ratio comparing to the existing microphone products on the market. Due to the compact packaging it occupies a small area as well.

Resumé

Emnet i denne afhandling er design af CMOS forstærkere for kondensatormikrofoner. MEMS (mikro-elektro-mekanisk) kondensatormikrofoner vinder stadig større udbredelse, fordi de er små, billige og lette at integrere med CMOS elektronik, hvorved der kan opnås ekstra funktionalitet og bedre performance. Imidlertid stiller denne kondensatortype øgede krav til interface elektronik, blandt andet på grund af mikrofonens støjegenskaber.

Mulige metoder for at detektere signalet fra en kondensatormikrofon er undersøgt og forklaret i denne afhandling. Den metode, som giver de bedste resultater mht. støj-egenskaber, er blevet valgt ved implementering af en eksperimentel forstærkerkonstruktion.

Forstærkerens egenstøj, især 1/f støjen ved lave frekvenser, er et betydeligt støjbidrag i det samlede system, og derfor er 1/f støjen i MOS transistorer undersøgt både teoretisk og eksperimentelt i projektet. Resultaterne heraf er præsenteret i afhandlingens del to, og i afhandlingens tredje del er de opnåede resultater anvendt til optimering af en forstærker for kapacitive sensorer.

I afhandlingens fjerde og sidste del beskrives et helt nyt forforstærkerdesign baseret på et koncept med to mikrofoner, som arbejder i modfase. Hermed opnås forbedrede støjegenskaber for det samlede system. Systemet er implementeret i en chip-scale pakke (CSP) med to mikrofonchips og en CMOS chip. Dette system resulterer i en mikrofon med flere dB bedre signal-støj-forhold end de eksisterende mikrofoner på markedet. På grund af den kompakte pakning, optager denne løsning kun et meget lille areal.

Acknowledgments

This thesis describes a three-year-and-four month work as Industrial PhD student in Pulse MEMS ApS (former Sonion) in collaboration with Centre for Physical Electronics at DTU Elektro. The study has been supported by Pulse (Sonion) and the Danish Ministry of Science (VTU) under the Industrial PhD Programme which is a remarkable initiative ensuring high prospects both for the industry and for research. I am grateful to both parts for investing in my education in this way.

Several people have been involved in this project. First of all I have to acknowledge Lars J. Stenberg, company supervisor, who has described and applied for this project besides being very actively involved in it and supporting all of its phases. He has initiated the design of a preamplifier for two microphones and I should thank him for any successful part of this thesis. I am also grateful to Prof. Erik Bruun without whom, I wouldn't literarily be able to start the project and even more importantly to finish it and for taking over the role of university supervisor in my second year of studies. I am thankful to Prof. Pietro Andreani for his supervision during the first year of this project, for his inspiring teaching and research passion and for help with the ISSCC conference. I acknowledge Pirmin Rombach who accepted to be the company supervisor in the last months of this project.

The longest period of this study has been spent in the IC department of Sonion (Pulse MEMS) and I would like to acknowledge all of my colleagues for their help and many discussions. Per F. Høvesten has introduced me to the general problems of a microphone preamplifier design, Gino Rocca was asked many times about the tools besides agreeing about my work during leave from PhD on our 'spicy' project. Jonas V. Nielsen has helped invaluably with his assembly proposal for the dual mic. Working with so good colleagues in our department was really a pleasure. From DTU I would like to thank Allan Jørgensen, who is invaluably helpful to all students, for providing a lot of software used during the project. I am also thankful to Prof. Maher Kayal from EPFL for accepting me as a guest PhD student.

I thank to all my friends, missing many of them who are spread around the world. I acknowledge my family for their support in everything I do, my husband, my sister and my parents. And thank to my niece Simona, a great happiness has been brought to all of our lives.

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1 Introduction

A large market exists for condenser microphones, with more than 2 billion of them produced annually. The design of condenser microphones is targeted towards applications in high volume consumer electronic products (mobile phones, cameras, headsets etc.). Condenser microphones will be briefly described in this thesis. As the signal from a microphone is typically small, they require an accompanying electronic circuitry that would provide amplification, impedance conversion and deliver the amplified signal to the following signal processing circuitry.

A topic of this thesis is the design of CMOS preamplifiers for condenser microphones. CMOS technology is a widely used technology, with its developments driven by the digital circuits billions of which are used in computers and other electronic equipment. To be able to integrate as many functionalities as possible without occupying a large area, transistor devices are getting smaller and smaller, with a minimum nowadays transistor channel length of 30nm. Minimizing the device size poses a challenge especially to analog circuit designers due to the fact that with the technology scaling accompanying decrease of the supply voltage is not followed by a proportional decrease in the transistor threshold voltage, what makes maintaining a high signal-to-noise ratio a difficult task. Besides that, a reduction in device size leads to increased $1/f$ noise.

A similar trend for having small electronic equipment, drives the development of condenser microphones, which are also shrunk to sizes which allow them to be integrated in for example thin mobile phones. This leads to their increased noise and poses even more stringent requirements to the amplifying circuits. Therefore, this thesis is devoted to investigating methods for an improved amplification of the microphone signal with respect to current developments in both technologies (condenser microphones technologies and the CMOS technology). As MEMS microphones are easy to integrate with CMOS, the CMOS electronics gains an increased importance because it can contribute to the overall improved performance of the system by extra functionalities (for example a digital output) that the circuits can introduce.

Due to the usually predicted exponential growth and a high potential of the microphone market, especially for MEMS (micro-electro-mechanical) condenser microphones, a lot of technology development is going on and there is a tough competition ongoing among the players in the industry that we are part of. In the light of that, the topic of this thesis is very relevant as the technological improvements (along with a reduced production cost) can lead to attaining and maintaining a competitive position.

Current Pulse's microphone products are comparable in performance to the other state-of-the-art microphones on the market and SiMic^{TM} [1] is still the smallest available silicon microphone. Its performance summary is shown in Table 1. It is designed to fulfill specifications when used on the telecom market (mobile terminals mostly) and the microphone membrane radius is $500\mu m$. Other MEMS microphone products have a similar performance and are targeted for the same market. As the existing company solution has already a competitive performance, a task to develop a better and or an original solution than it during this project is not an easy one. In the Table 1 we show also the specifications for microphones used on the hearing instruments market, which is still covered by the high quality electret microphones.

Property	Unit	SiMic (Telecom Applications)	Hearing Instruments
Size	mm^3	2.33×1.6×0.865	
Sensitivity	dBV@1Pa, 1kHz	-40	-33
SNR	dB@1Pa,A-weighted	61	68
Response	Hz	20-20k	100-10k
V_{sup} (range)	V	1.8 (1.64-2.86)	0.9-1.5
I_{sup}	μA	330	50
PSRR	dB	>60	>20
THD	%@dB SPL, 1kHz	2@104	1@120
R_{out}	Ω	500	

Table 1: Summary of properties of Pulse's SiMic [1] (standard for telecom applications) and specifications for a hearing instrument microphone.

One of the key properties is that the MEMS microphones are designed with a relatively small membrane not allowing a very high signal-to-noise ratio. So a desired goal of this project is to design an amplifier that would lead to an improved performance of the microphone comparing to properties for telecom application summarized in the Table 1, i.e. to make it closer to fulfilling the specifications for hearing instruments, the most important of them the signal-to-noise ratio.

In the first part of this thesis, possible microphone signal sensing methods have been explained and compared in order to investigate which of them would be the best to use as an interface to our microphone. Due to the fact that the electronics noise performance is an important factor for the overall noise of the system, and because in the start of this project a technology with a poorly characterized CMOS transistor flicker noise has been used in the company, the investigation of $1/f$ noise in CMOS has been done and is explained in the second part of the thesis. In the third part, the knowledge about the transistor noise previously obtained has been applied to a problem of optimization of an interface for a capacitive sensor. Finally, in the fourth part, a novel preamplifier designed demonstrating a concept of a differential operation of two microphones biased with voltages of opposite polarities [2] has been described. The amplifier shows how accompanying electronic circuitry can be used to enhance performance of MEMS microphones and in Fig. 1 a new enhanced performance microphone chip-scale package (CSP) with two microphone dies and the CMOS amplifier is shown with an Euro. With the performance improvement due to the use of two microphone dies (a larger membrane area) that our amplifier allowed new potential markets are a step closer.

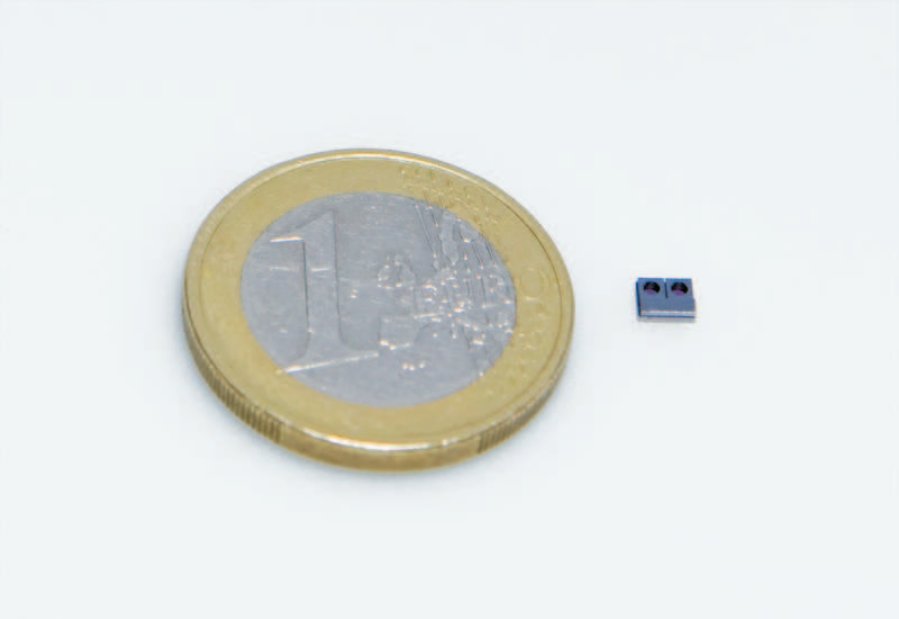

Figure 1: A microphone chip-scale package developed in this project comprising the amplifier and two MEMS dies beside one Euro coin.

References

[1] *Datasheet of Pulse TC200A SiMic^{TM} Analog Silicon Microphone*, 2008.

[2] A. van Halteren, "Microphone with Dual Transducers," *Patent application US 2008/0192962 A1*, filing date 12/Feb/2008.

2 Condenser Microphones

Microphone is a transducer that converts acoustical energy (sound) into electric energy (electric signal) [1]. A microphone type consisting of two parallel plates forming a capacitor is called condenser, capacitor or electrostatic microphone. One plate of the capacitor is a fixed, rigid backplate, filled with holes allowing movements of the air, while the other is a movable diaphragm. Sound vibrations produce changes of the distance between the microphone capacitor plates changing the value of the microphone capacitance C_m.

The microphone capacitance is given by

$$C_m \quad = \quad \varepsilon_0 \cdot \frac{A}{d} \tag{1}$$

where ε_0 is the permittivity of vacuum, A and d are a capacitor plates area and a distance between the plates respectively. A change in the capacitance is thus $\Delta C_m = C_m \frac{\Delta d}{d}$. This change can be detected or sensed in several ways and needs to be amplified to obtain a measurable signal.

As the voltage V on the capacitor C_m with charge Q is given by $V = \frac{Q}{C_m}$, when the charge on the microphone is kept constant $\Delta C_m = C_m \frac{\Delta V}{V}$ i.e. a change of the microphone capacitance can be detected by sensing the voltage from it, ΔV. The microphone sensitivity, S, then expresses the change in the voltage of the microphone in response to applied sound pressure (V_{rms} per Pascal at 1kHz) and is given by

$$S = \frac{\Delta V_m}{\Delta P} = \frac{V_b}{Cm} \cdot \frac{\Delta Cm}{\Delta P} = \frac{Vb}{d} \cdot \frac{\Delta d}{\Delta P} \tag{2}$$

A microphone bias voltage is called V_b in the latter formula. A condenser microphone in a constant charge mode can be represented by an equivalent electrical circuit consisting of a voltage source, i.e. output from the microphone when a sound pressure is applied V_m in series with its capacitance C_m.

The transduction behavior of a condenser microphone can be predicted by looking at its acoustical and electrical behavior. Mechanically the microphone presents a spring mass system where its displacement, d, is caused by the sound pressure P on a membrane area A and can be be expressed by

$$F = \frac{P}{A} = kd \tag{3}$$

k is a membrane spring constant [2]. A microphone resonant frequency is $\sqrt{\frac{k}{m}}$, m is the mass attached to the spring, and the resonant frequency should be larger than the upper audio band frequency of 20kHz.

The acoustical behavior of a condenser microphone can be modeled by a lumped-parameter electrical equivalent circuit. In that analogy a sound pressure p (deviation from the ambient atmospheric pressure) is analogous to a voltage in an electrical equivalent circuit and a volume velocity U (a volume of the air moved per unit time) corresponds to an electrical current [3]. An acoustic impedance is then defined as pressure over volume velocity ($Z = p/U$). Acoustic compliances which are a measure of a membrane stiffness are modeled as capacitors, air-mass as inductance and dissipative effects as resistors [4]-[5]. Similarly to the thermal noise in electric circuits the acoustic resistances generate an acoustic noise. Microphone noise is an important microphone parameter and is expressed in dB(A) SPL, i.e.

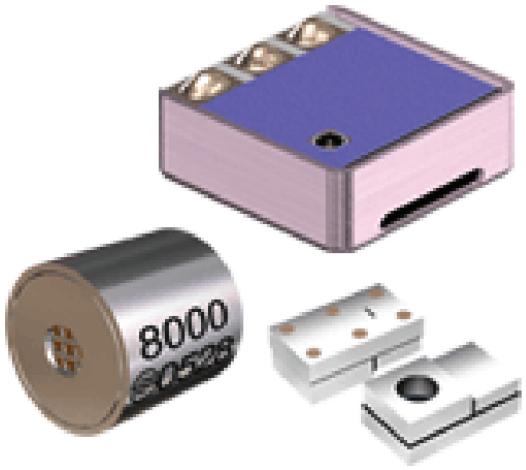

Figure 2: Pulse's condenser microphones: ECM and MEMS (the smallest one).

decibels relative to 20μ Pa sound pressure level (SPL) where the noise power spectrum is A-weighted [6].

Two types of electret condenser microphones exist and will be shortly described: permanently charged electret condenser microphones (ECM) and MEMS (microelectromechanical) microphones which are externally biased. In Fig. 2 as an illustration these two types of microphones are shown, a MEMS microphone is the smallest on the figure with its footprint of $1.6mm \times 2.6mm$ and below one millimeter in hight.

2.1 Electret Condenser Microphones (ECM)

Electret microphones are condenser microphones that use electret, permanently electrically charged, or polarized ferroelectric material to provide a charge on the microphone capacitor. A charge from the electret corresponds to a microphone bias voltage of several hundreds of volts and will not decay for long time if used under non-extreme conditions. The electret can be implemented in several ways (for example deposited on the membrane or on the backplate), however, the electret condenser microphones have been in use in principle unchanged for the last 50 years.

A preamplifier traditionally used with electret microphones consists of a JFET transistor buffer. With the advent of CMOS technology JFET has been replaced by a CMOS transistor. The electret microphone itself is charged and it doesn't need an external bias voltage while its amplifier needs a supply voltage.

Electret microphones are sometimes considered low-cost and low quality microphones, but it should be pointed out that their reputation of low quality performance microphones is due to the demand to produce electret cheaply and not because of the inherent limitations of the electret. The best electret microphones show a very competitive performance. The air gap of an ECM microphone is tens of microns and its capacitance can be from below 1pF to some tens of pF. The sensitivity of an ECM is 5-20$\frac{mV_{rms}}{Pa}$.

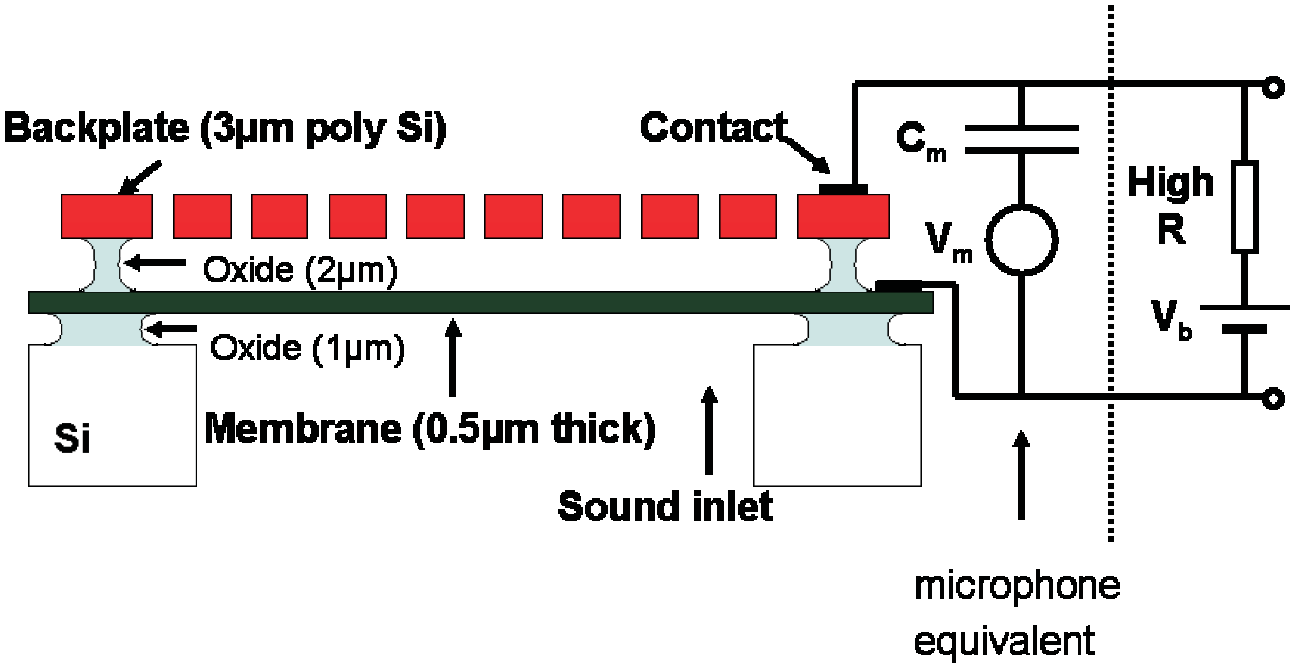

Figure 3: A MEMS microphone die cross section and a microphone equivalent circuit.

2.2 MEMS Microphones

MEMS microphones are a relatively new application of MEMS i. e. micro-electro mechanical technology with their development started in mid-nineties [1]. The first MEMS microphone products on the market appeared about a decade later and it is still relatively new and not as mature technology as CMOS. MEMS microphones consist of a stiff backplate with damping holes, and a flexible membrane as shown in Fig. 3. The damping holes let the air flow through the backplate and act as a buffer balancing the pressure difference when the membrane moves.

A MEMS microphone capacitor plates are built on the top of a silicon wafer by using MEMS technology that allows creation of small mechanical structures on the surface of a silicon wafer. Similarly to creating semiconductor devices in silicon, MEMS microphone capacitor plates are formed from a silicon wafer by deposition and removal of semiconductor materials. Two MEMS technologies exist: bulk micromachining that is used to etch structures on silicon, and surface micromachining that involves depositing layers of polysilicon to create structures. Both of them are used for creation of Pulse's silicon microphone which is shown in Fig. 4; on the left a MEMS microphone die with $500\mu m$ radius is shown when looking into its backplate and to the right a cross-section of a MEMS microphone with removed membrane, where it is possible to see the microphone sound inlet (membrane is normally placed where the sound comes from) and the microphone back-chamber. The back chamber is part of the silicon substrate that the microphone die is flip-chip mounted to. Thickness of the membrane is 0.5 μm.

Contrary to an ECM, a MEMS microphone needs an external bias voltage that will provide charge between the plates. That charge is normally generated by an external bias voltage generated on-chip from a power supply by a CMOS circuit called voltage pump, charge pump [7] and can be removed

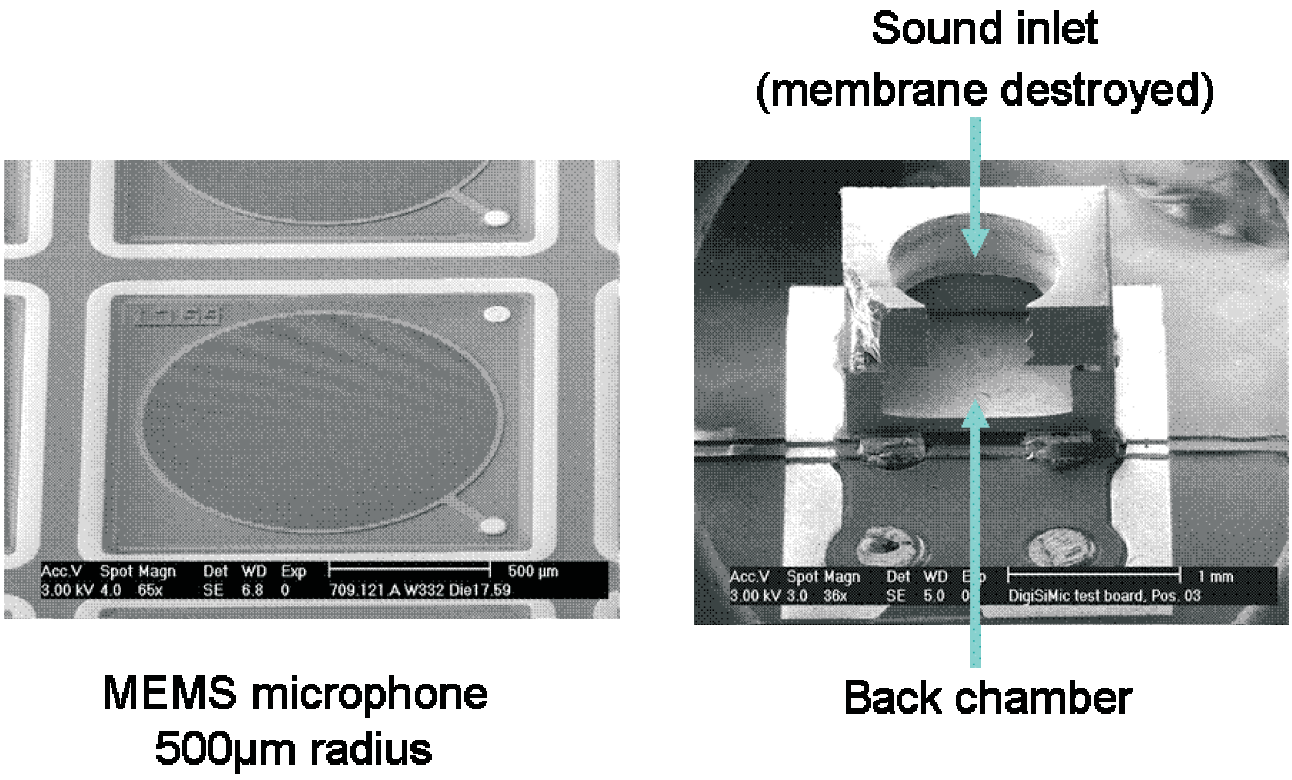

Figure 4: Left: Pulse's MEMS microphone die looking into its backplate. Right: A cross-section of the chip-scale package with removed microphone membrane.

during microphone inactivity. In Fig. 3, the external bias voltage is denoted V_b. A first approximation microphone equivalent circuit (V_m in series with C_m) is shown in Fig. 3 as well. More detailed, parasitic capacitances and resistors have to be taken into consideration. In the microphone used here, a leak resistor exists between the membrane and the backplate and between the backplate and the substrate and there are parasitic capacitances between the membrane and the substrate and between the backplate and the substrate.

Microphone sensitivity increases with microphone bias voltage (2) and the nominal bias voltage for the microphone used is around 10V. Capacitance of the microphone used is around 5pF. The air gap of MEMS microphones is smaller than ECM, it is a couple of micrometers, as the voltage of ECM is much larger than the voltage of a MEMS microphone. Sensitivity of MEMS microphones is typically 3.5-10$\frac{mV_{rms}}{Pa}$

Tradeoffs in the design of MEMS microphones are numerous, for increasing the microphone sensitivity low stiffness of the membrane is needed as well as a thin membrane. On the other hand, the resonant frequency of the microphone should be above 20kHz and therefore the designed structure can not be too soft. The membrane has some residual stress and the microphone packaging is also a source of residual stress and both need to be taken into consideration. Another phenomenon related to the microphone membrane is its collapse or pull-in voltage. With increased bias microphone sensitivity increases and the membrane deforms until this critical voltage is reached and after that the growth of electrostatic forces between the capacitor plates due to the bias voltage becomes dominant over the

Design Parameter	Low Value	High Value
Membrane Mechanical Stress	+ low noise - collapse	+ low distortion and high SPL -high noise level
Air Gap Thickness	+ low bias voltage needed - collapse	+ low distortion and high SPL -low capacitance and high loss

Table 2: An example of tradeoffs in the design of MEMS microphones [4].

linearly increasing mechanical restoring forces [4] and the membrane quickly sticks to the backplate. For restoring a proper operation again, the microphone needs to be discharged to zero Volt, which can be done by a circuit such as the one described in [8].

Microphone sensitivity increases with an increased microphone area, but a small area is desired because of the requirement for low microphone price and demands on the market for devices that can be placed in a small volume. Therefore, a MEMS microphone diaphragm is usually below 2mm. With a decreased microphone area microphone noise increases and for MEMS microphones, microphone thermomechanical noise even dominates noise of the accompanying electronic circuitry [9]. Microphone signal-to-noise ratio (SNR) is a microphone signal (1kHz@1Pa) divided by the microphone A-weighted noise and is constant as a function of bias. In [10] it has been shown that lower noise and higher sensitivity can be achieved with a smaller membrane areal density (membrane mass per unit area).

A small microphone area is a good property concerning its frequency response due to the fact that the microphone is much smaller than the smallest audio band wavelength (17mm). The influence of the microphone package on the frequency response should be taken into consideration as well. For the microphone used here the lumped element model with analytical expressions for all of its acoustical elements exist as internal data as well as a full microphone equivalent electrical circuit, but a detailed study of the condenser microphone is beyond the scope of this project. Just as an illustration of the microphone design task, some of the design trade-offs are shown in Table 2 based on internal data [4]. An electrical model of the microphone has been used for simulations during circuit design.

MEMS microphones are very suitable for integration with electronics and besides a CMOS preamplifier are often supplied with an A/D converter providing a digital output. There are ongoing discussions in the MEMS community about the advantages of integrating CMOS circuitry and MEMS microphone on the same die. At the moment most of the manufacturers produce separate dies and the price of a completely integrated solution might still be higher, design time longer and yield reduced comparing to a separate dies solution [11]. So majority of nowadays MEMS microphones solutions [12]-[17] consist of two dies: a MEMS microphone die and a CMOS amplifier die connected with bond wires and placed in a Faraday cage (covered with a lid) with a standard size $4.72 \times 3.76 \times 1.25 mm^3$. [18] offers a solution with a MEMS die and a CMOS die without the inter-die wirebonds in a standard CMOS package that occupies $2mm \times 2mm$.

Pulse's microphone products [19] are packaged using a chip-scale packaging technique (CSP) consisting of the MEMS microphone chip and the CMOS chip that are flip-chip mounted onto a silicon

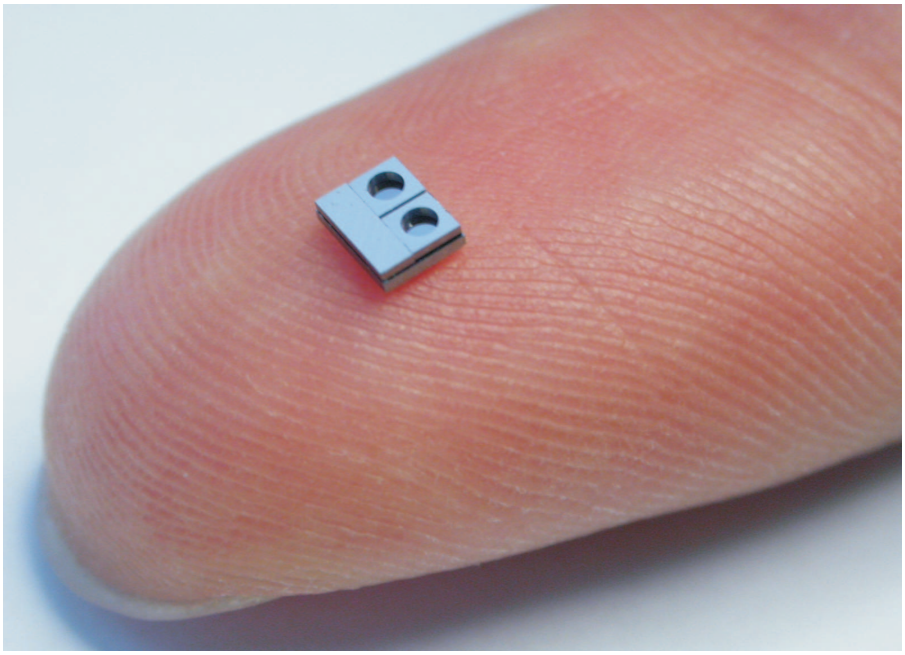

Figure 5: A new microphone with two MEMS dies developed in this project: the size of its chip scale package (CSP) is 2.6mm×3.2mm×0.865mm.

substrate. Contacts between the microphone and the amplifier in the CSP are provided through connections on the substrate with minimal parasitic capacitances. Pulse's analog microphone $SiMic^{TM}$ CSP occupies $2.33mm \times 1.60mm$ only and it has long been far the smallest among all the other MEMS microphones on the market. In Fig. 5 a chip scale package for two microphone dies that has been developed as a part of this project is shown. It occupies a double size of a Pulse's digital microphone product with dimensions 2.6mm×1.6mm×0.865mm and shows a very competitive signal-to-noise ratio as it will be explained in this thesis.

2.3 MEMS Microphones on the Microphone Market

More than 2 billion microphones are produced annually, most of them of ECM type, and 650 million of them is used in cell phones only [20]. The number of microphones produced is growing end the development is driven by a wish for better performance in mobile communications, and therefore multiple microphones solutions combined with associated signal processing are gaining interests. However, the component price is a key factor on the high volume electronics market and the microphone price is set by Asian suppliers of low-cost ECM microphones [11], so despite the advantages, to attain own share of the market, MEMS microphones need to be both price and performance competitive.

During the last decade, MEMS technology has found its application in a number of industries. One example are MEMS accelerometers widely used for airbags in the automobile industry. Target markets for MEMS microphones are high volume consumer electronics products such as mobile phones, cameras, PDAs (personal digital assistant), headsets etc. The size of cell phones has continuously been getting smaller and the number of new features increasing requiring smaller components and components that

can be integrated. ECM microphones for portable devices are typically 6mm in diameter and the smallest ones have been shrunk down to 4mm, with height 1-2mm [21]. Further size reduction will lead to reduced performance in sensitivity, frequency response and noise and is unlikely to happen as the technology limits have been reached.

MEMS microphones are significantly smaller than the smallest ECM and that is one of the reasons stimulating the development of MEMS microphones. They fill up less area and are significantly thinner what allows them to be mounted in modern thin mobile phones. Another driving force for the use of MEMS microphones is that they can be surface mounted. Comparing to them, the electret of the ECM microphones can not withstand high reflow temperatures and they are mounted in a socket that is soldered to a circuit board. MEMS microphones are sometimes even addressed as 'reflow mics' because of their solder mounting. An advantage of the surface mounting is that an automatic pick-and-place equipment is used what contributes to cost savings. The third advantage of MEMS microphones over ECM is that the MEMS technology is compatible with widely used CMOS electronics and the two can be easily integrated leading to an enhanced performance of the microphones and the microphones with new functionalities such as a digital output. Using MEMS microphones eases applications with multiple microphones on a singe chip as well allowing directionality.

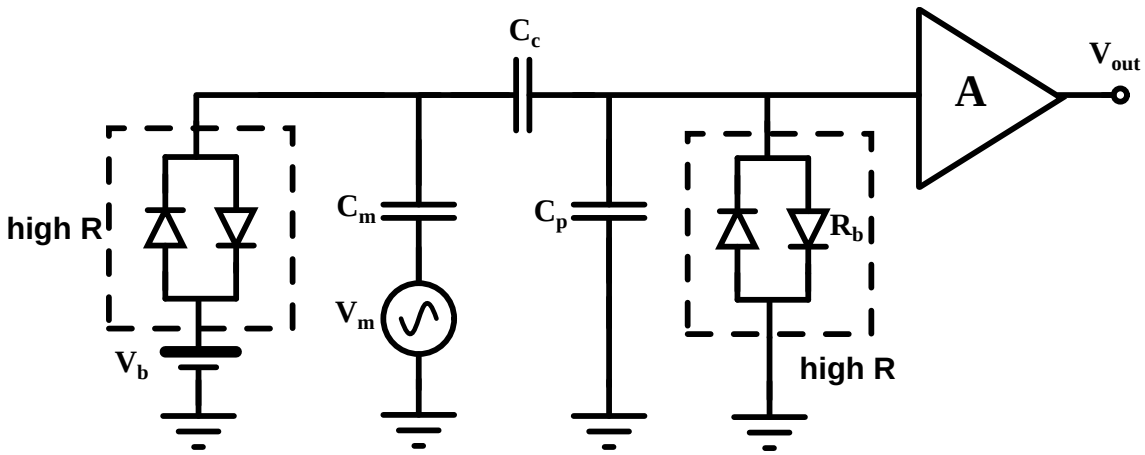

Figure 6: MEMS microphone voltage sensing principle.

3 Condenser Microphone Sensing Principles

3.1 Constant Charge, Voltage Sensing

When the charge of a condenser microphone is kept nearly constant and as the capacitance changes due to the incoming sound wave this change will be reflected in the change of voltage across the capacitor. This voltage change needs to be amplified and the microphone is, as shown in Fig. 6, connected to the input of an amplifier. To provide a DC path to ground at the amplifier input a very high resistor is needed and can be implemented in several ways. A traditional solution is using diodes as shown in Fig. 6. The capacitance of the microphone C_m and the bias resistor R_b form a high pass filter and the transfer function is

$$A(s) = \frac{V_{out}}{V_m} = A\frac{C_m}{C_m + C_p + C_{in}} \frac{s}{s + \frac{1}{R_b(C_m+C_p+C_{in})}} \tag{4}$$

The cut-off frequency given by $\frac{1}{R_b(C_m+C_p+C_{in})}$ should be well below the lower frequency of the audio band (with C_m=5pF, a cut-off frequency below 20Hz is obtained with R_b larger than 1.6GΩ). C_p is a parasitic capacitance that might exist from the interface node to ground and C_{in} is the amplifier input capacitance. C_c is a large capacitor used for DC decoupling of the MOS circuit from the high microphone bias voltage. The amplifier gain A is close to one for a source-follower and $G_m R_{out}$ for a common-source and OTA amplifiers (G_m and R_{out} are the amplifier transconductance and the output resistance respectively).

The resistor used for biasing has to be very large also not to influence the noise performance of the microphone. Any leakage current and the parasitic capacitance at the sensitive high-impedance microphone-preamplifier interface node is undesirable as they lead to an increased noise and a reduced output sensitivity. These are some of the critical issues making the design of a microphone preamplifier a challenging task. Clearly due to these issues packaging and interconnection of the microphone sensor is of crucial importance. In Fig. 6 it is assumed that a MEMS microphone is used, as its bias voltage V_b is shown; for an ECM microphone, a principal schematics would be the same just without the bias

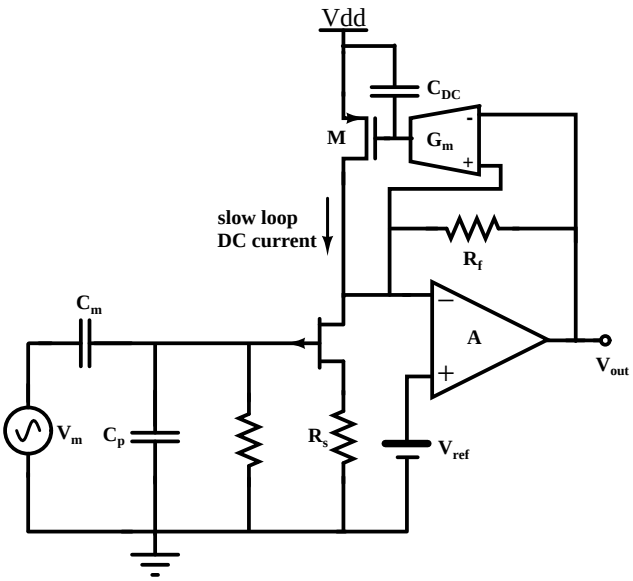

Figure 7: The current from a JFET with an ECM is sensed to improve PSRR in [30].

voltage and with the microphone capacitor plate connected to ground.

The noise of the system can be calculated by including the noise models for the amplifier, microphone and the resistor [22] (will be discussed in details in this thesis), and neglecting the bias resistor R_b input noise power spectral density (PSD) ($\frac{4kT}{R_b\omega^2C_m^2}$), the signal-to-noise ratio (SNR) is

$$SNR = 20 \cdot log \frac{V_m}{\sqrt{V_{n,m}^2 + V_{n,in,amp,rms}^2 \left(\frac{C_m+C_p+C_{in}}{C_m}\right)^2}} \tag{5}$$

where V_m is the microphone signal, $V_{n,m}$ the microphone noise and $V_{n,in,amp,rms}$ the input referred noise of the amplifier. As a single ended input amplifier (a single transistor interfacing the sensor) has minimal noise [23], the highest SNR can be achieved by using it.When calculating the SNR, microphone voltage and microphone noise values are in rms units. They are per default specified in this way.

As an example we can calculate the SNR using (5) with the following data: microphone output signal $V_m = 4.2\frac{mV_{rms}}{Pa}$, microphone noise $V_{n,m} = 2.5\mu V_{rms}$, $C_m + C_p \approx C_m$ and amplifier input referred noise including its thermal and flicker noise contribution in the the A-weighted audio band $V_{n,in,amp,rms} = 0.7\mu V_{rms,A}$. Knowing that the amplifier is optimally biased when its input capacitance C_{in} is close to $C_m + C_p$ we get SNR=63.3dB. The SNR with zero microphone noise is 69.4dB. Current consumption for the transconductance chosen is below $100\mu A$. As an important fact, we mention that the transistor rms noise $V_{n,in,amp,rms} = 0.7\mu V_{rms,A}$ used in calculations is close to the limits of nowadays CMOS technologies what will be shown in this thesis.

The amplifier in the voltage sensing solution can be a differential amplifier or a single transistor amplifier. Most commonly used solution for ECMs was a JFET source follower. Examples of microphone preamplifiers using a JFET can be found in [24]-[25]. In [24] an ECM microphone is connected to the input of a single JFET source follower and in [25] a quasi differential structure has been used, where the first stage, a branch with a microphone amplified by a JFET is duplicated with a dummy

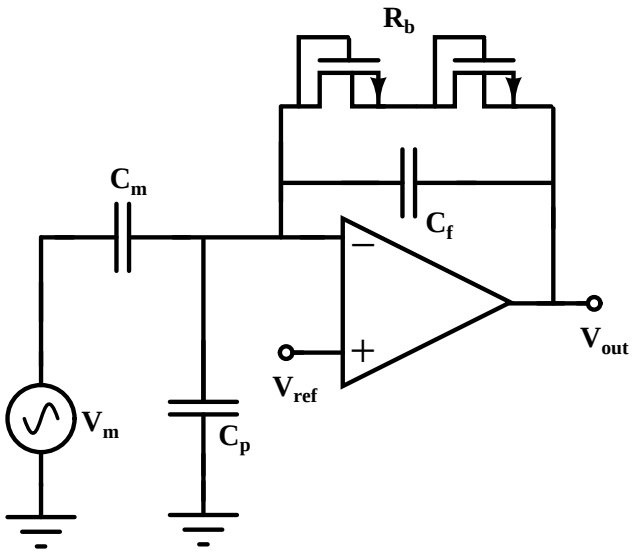

Figure 8: A typical capacitive feedback amplifier, DC biasing is provided by diode connected transistors.

capacitor at the second input and the outputs of the two branches are fed to the inputs of a differential bipolar amplifier. In both examples diodes are used as resistors. One of disadvantages of a JFET is its leakage current which is in the order of $10^{-9}A$ and increases with temperature. Other disadvantages are a low voltage gain and large variations of IDSS from one device to the other. Majority of nowadays integrated circuits are made using submicron CMOS technology and JFET is practically obsolete.

A single transistor CMOS source-follower amplifier implementations for an ECM can be found in [26]-[27] using diodes or diode-connected transistors for biasing the input transistor. In [7], [28] MEMS microphones are interfaced with a CMOS source follower. A single transistor implementation is preferable solution for achieving low-noise, but as it is known that it has a low power supply rejection, attempts have been made for its PSRR improvements. In [29] PSR of an ECM amplifier is enhanced by stacked depletion devices and in [30] PSRR is improved by sensing and amplifying a current of a JFET amplifier of an ECM by an additional CMOS circuitry as shown in Fig. 7. The DC voltage drop in the feedback load R_f is proportional to the DC output current of the amplifier and is regulated to zero by canceling the microphone buffer's DC current with the feedback DC current from the transistor M. This feedback loop is slow as is the microphone bias current and as the slow DC currents are subtracted from each other, only AC current is sensed by the fast amplifier A.

Differential CMOS preamplifiers for an ECM are described in [31]-[32] and in [33] for a MEMS microphone all having a single ended output and with a standard diode biasing. In [34] g_m of an OTA is used as a high resistor for biasing and the following OTA used for amplification provides a differential output current of the ECM preamplifier. In [35]-[36] a DDA (differential difference) amplifier with two differential inputs and a single ended output has been used [37] where the first input is used for amplifying the signal from the ECM and the second for providing the DC voltage at the output of the amplifier.

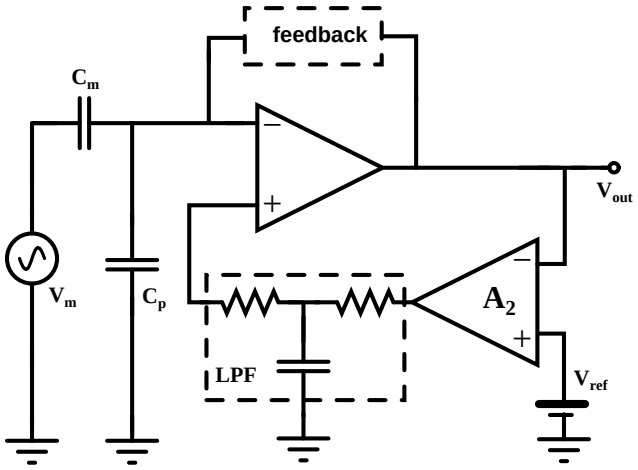

Figure 9: Microphone preamplifier with two loops. The feedback loops sets the DC output voltage and provides a non-zero DC voltage at the main amplifier input.

For providing a well defined gain, increase in bandwidth, and a controlled input/output impedance, amplifiers are typically used with a feedback [38]. A commonly used capacitive feedback voltage amplifier shown in Fig. 8 is used among other for neural recording applications [39]. Biasing of the output is done by using two MOS bipolar elements presenting a resistor R_b. The transfer function of the circuit is

$$A(s) = \frac{V_{out}}{V_m} = \frac{-sC_m}{C_f\left(s + \frac{1}{C_f R_b}\right)} \approx -\frac{C_m}{C_f} \tag{6}$$

where C_f is the feedback capacitor. The signal-to-noise ratio is

$$SNR = 20 \cdot log \frac{V_m}{\sqrt{V_{n,m}^2 + V_{n,in,amp,rms}^2 \left(\frac{C_m + C_p + C_{in} + C_f}{C_m}\right)^2}} \tag{7}$$

which is lower than (5) and depends on the C_f value chosen for the desired gain. The resistor noise should be added and is the same as in the previous case; C_{in} is the amplifier input capacitance. The cut-off frequency of the amplifier ($\frac{1}{C_f R_b}$) determined by the bias resistor has to be lower than 20Hz.

In the neural recording application design from [39] the THD at the output is 1% for 16.7mV_{pp} input signal (and gain 40dB) and as the typical signal from the microphone for the maximum sound pressure level is much larger than this value (20 times the microphone output voltage for 1Pa input SPL, i.e. 20 times $4.2\frac{mV_{rms}}{Pa}$), it can be expected that the THD would be rather high if the same amplifier was used as a microphone preamplifier. A similar explanation for not using this basic topology as a microphone preamplifier in voltage sensing can be found in [40] where it is explained that if a diode was used to set the DC level of the output, the signal on the output would be seen directly by the diode and at the amplifier input and a severe nonlinearity would be produced. This has been confirmed in our simulations, although not much time has been devoted to investigating if a solution for using this topology can be found.

For these reasons in [40] a two-feedback solution has been proposed, one extra feedback was used for setting the DC voltage at the amplifier output (called servo feedback) and providing a low-frequency

cut-off along with a standard capacitive feedback, what evolved to a solution with a DDA in [35]. A similar solution has been explained in [31] and is shown in Fig. 9 where the main amplifier amplifies the signal from the microphone and the feedback amplifierA_2 provides the DC voltage at the output. With the DC bias feedback loop shown, higher voltages than zero Volt can be established at the gates of the preamplifier input transistors; to obtain a proper frequency response (cut off frequency below 20Hz and a flat frequency response in the audio band), a filter structure similar to the one shown in Fig. 9 is needed at the output of the feedback loop. The resistors in the filter structure are large and can be implemented by using back-to-back diodes as suggested in a similar topology in [41].

Due to large resistor values, microphone preamplifiers are prone to a long start-up time [31], [40] and [41] and must be carefully designed. Care should be taken about the THD of these circuits especially when using non-linear devices such as diodes as well. Using a differential amplifier for signal amplification it is possible to achieve enhanced amplifier performance, however a single transistor amplifier as an interface to the microphone is sometimes preferable because of lower noise. In [42] a design of a $\Delta\Sigma$ modulator interface for an ECM is described.

3.2 Constant Voltage, Charge Sensing

Preamplifiers described by now can be used for sensing a microphone output in a constant charge mode, that is its open-circuit voltage. If an electret microphone inputs are short-circuited it is possible to sense its short-circuit current, that is the microphone is in a constant voltage mode. Amplifiers operating on a current level in BIMOS and Bipolar technology from [43]-[44] are used as preamplifiers for electret microphone when the current sensing principle is used (short-circuit current sensed).

A similar method for a read-out of a capacitive sensor, when its voltage is constant, is the charge-change sensing using a so called charge amplifier ($\Delta Q = V_b \Delta C_m$). Charge sensitive amplifiers are used for interfacing CCD (charge-coupled imaging devices), radiation detectors and other. A low-noise performance is a critical issue in designing such amplifiers and they are described in general in [45], in [46] in connection with a differential micromechanical capacitive gyroscope and in [47] for a micromachined ultrasonic transducer. A design of a charge amplifier interfacing a MEMS microphone is described in [48]-[49] and will be explained here.

In all charge amplifier applications a voltage over the sensor has to be kept constant and in [48] this is done by a MOS bipolar feedback element (low cut-off frequency is $\frac{1}{C_f R_b}$) in the same way as shown in Fig. 8 and by using a floating-gate amplifier [50]-[51] in the solution for a capacitive ultrasonic sensor. However for the MEMS microphone in the same work and using the same floating gate amplifier topology a charge adaptation scheme using Fowler-Nordheim tunneling and channel hot-electron injection mechanism [52] has been used for stabilizing the output DC voltage providing at the same time the cut-off frequency of 0.2Hz.

The charge-sensitive amplifier from [48] is shown in Fig. 10 along with the floating node charge adaptation circuit consisting of a tunneling junction and an indirect injection pFET transistor. Formulas for a charge amplifier circuit analysis explained in [48]-[49] will be shown here. The DC voltage

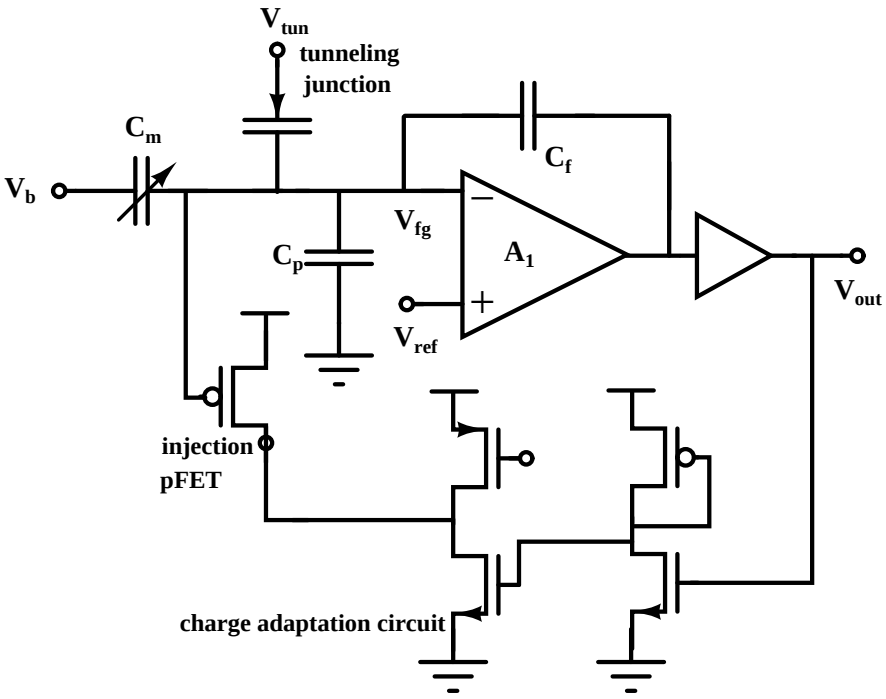

Figure 10: MEMS microphone charge sensitive amplifier with the charge adaptation circuit from [48].

of the charge amplifier is

$$V_{out} = -\frac{V_b C_m + Q}{C_f(1+\rho)} \tag{8}$$

where $\rho = \frac{C_T}{C_f A_1}$, $C_T = C_m + C_p + C_{in}$, C_{in} is the amplifier input capacitance, A_1 is the amplifier open loop gain $A_1 = G_m R_o$, G_m and R_o are the amplifier transconductance and the output resistance respectively and Q charge on the floating node. The factor $1+\rho$ is due to the non-ideality of the opamp and when $A_1 >> \frac{C_T}{C_f}$, $V_{out} \approx -\frac{V_b C_m + Q}{C_f}$. Therefore, the output DC voltage can be set at midrail by either adjusting the non-inverting terminal voltage if the floating-gate charge is fixed, or by adjusting the floating gate charge according to the output voltage. It is further explained in [48] that without the charge adaptation scheme, the adjustments can be done from outside although that is not stable as the floating nodes are very sensitive causing the output to saturate. It can be seen that the output from the charge amplifier increases with increased bias voltage V_b and decreased C_f.

The transfer function is calculated as

$$A(s) = \frac{V_{out(s)}}{C_m(s)} = -\frac{V_b}{C_f\,(1+\rho)} \cdot \frac{1 - s\frac{C_f}{G_m}}{1 + s\tau} \tag{9}$$

The time constant of the circuit is $\tau = \frac{C_{eff}}{G_m(1+\rho)}$, $C_{eff} = \frac{\left(C_o C_T - C_f^2\right)}{C_f}$ and $C_o = C_L + C_f$. Usually, C_f is much smaller than the load capacitance C_L and than the C_m. The pole frequency $(\frac{G_m}{C_{eff}})$ is larger than 20kHz and the frequency of zero due to the feedback capacitor is much larger than it. It is reported that the effective feedback resistance caused by the charge adaptation scheme is around $10^{12}\Omega$ and the lower cut-off frequency due to it is much below 20Hz. Thus the time constants of the charge amplifier approach are large similarly to when voltage sensing of the microphone is used. For a high amplifier

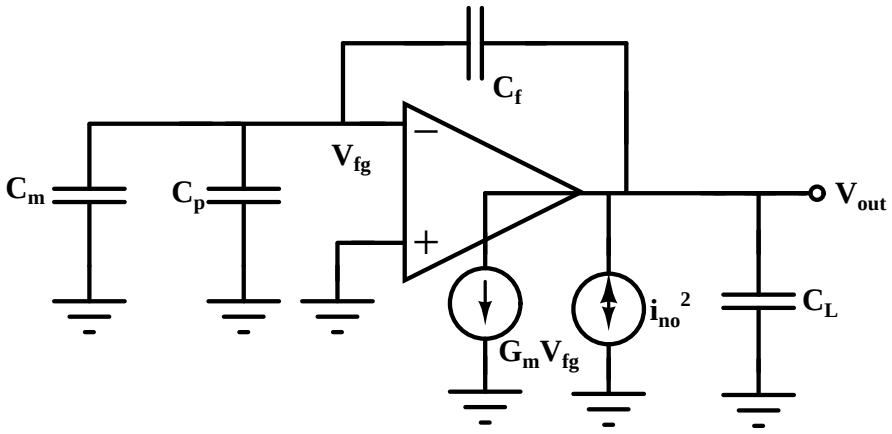

Figure 11: A small-signal model of the charge amplifier for noise analysis.

gain

$$A(s) = \frac{V_{out(s)}}{C_m(s)} = -\frac{V_b}{C_f} \cdot \frac{1 - s\frac{C_f}{G_m}}{1 + s\frac{C_{eff}}{G_m}} \tag{10}$$

Using the schematics shown in Fig. 11, the output noise power spectral density of the charge amplifier can be calculated as

$$V^2_{n,out}(f) = \left(\frac{C_T}{C_f G_m}\right)^2 \cdot \frac{i^2_{no}}{1 + \left(2\pi f \frac{C_T}{C_f G_m}\left(\frac{C_T C_f}{C_T + C_f} + C_L\right)\right)^2} \tag{11}$$

and it is further more integrated in the whole band from dc to infinite frequency (assuming that the thermal noise is dominant) giving an rms value equal

$$V^2_{n,out,rms} = \frac{i^2_{not}}{4G_m} \cdot \frac{C_T}{C_o C_f} \tag{12}$$

where i^2_{not} is the amplifier output thermal noise. The same result has been obtained in [53] in connection with the noise analysis of switched capacitor circuits. Further more, in [48] a maximum output voltage for a linear operation of the amplifier is calculated assuming that the input differential pair of the amplifier operates in weak inversion, which is equal $\Delta V_{out,max} = \frac{C_T}{C_f} 2U_T\eta$ where U_T and η are the transistor thermal voltage and the weak inversion slope factor respectively. Then the maximum dynamic range for a linear operation in [48] is given as

$$DR \approx \frac{16U^2_T G_m \eta^2}{i^2_{not}} \cdot \frac{C_L C_T}{C_f} \tag{13}$$

Using (10) and (12) we can calculate the signal-to-noise ratio ($20 \cdot log(\frac{V_{out}}{V_{n,out,rms}})$) neglecting the microphone noise for simplicity as

$$SNR = \frac{V_b \Delta C_m}{V_{int}\sqrt{\frac{G_m C_T C_f (1+\rho)}{4C_o}}} \tag{14}$$

where V_{int} is the amplifier input referred thermal noise.

For comparing this approach to the voltage sensing approach we can calculate the SNR with the following data: a capacitance change ΔC_m of the microphone is $\frac{2.3fF}{Pa}$, V_b=10V, $G_m = 500 \cdot 10^{-6}S$, $V_{int} = \sqrt{\frac{4kT}{G_m}}0.6\mu V$, $C_f = 200fF$, $C_T = 12pF$ and $C_L = 5pF$; using (14) the resulting SNR is 36.4dB when only thermal noise is taken in consideration. As the SNR for a microphone is usually calculated with A-weighted noise contribution, we have done re-integration of (11) in the audio band including the A-weighting filter using Maple and the SNR obtained in this way is 51dB; again with thermal noise only. Clearly the SNR would be lower if the flicker noise contribution was added. In the example with the voltage sensing amplifier flicker noise was included in the total noise of the transistor. Choosing another relation between the C_{in} and $C_m + C_p$ might give a bit better SNR, but this analysis anyhow shows that the SNR using a charge amplifier with a capacitive feedback is much lower than when using a voltage sensing method. This is in line with the table summarizing the results from literature shown in [48]. The work presented there has though a very low current consumption.

The amplifier of the charge amplifier in the analysis can be a simple cascode operational transconductance amplifier (OTA) (used in [48]), a folded cascode amplifier or a cascode common-source amplifier. For two stages amplifier, the dominant pole depends on the compensation capacitance and the power consumption is larger. Another example of a charge amplifier is described in [45] with a single-ended input folded cascode amplifier for detection of fast current pulses. In that application and in switched capacitors charge amplifiers, a reset switch is used in parallel with the feedback capacitor to reset charges on the nodes.

3.3 Capacitance Change Sensing

We can notice that in the previous two detection methods, a bias voltage is provided to the microphone, increasing the value of a detectable output signal. In the first case the output signal sensed is a voltage equal $V_b\frac{\Delta C_m(t)}{C_m}$ and in the second case the output voltage sensed is the microphone charge equal $V_b\Delta C_m(t)$. The third method is to sense the capacitance of the microphone i.e. $\Delta C_m(t)$.

If a microphone is a part of an LC tank oscillating system (Fig. 12), its capacitance carrying a sound message $C_m(t) = C_m - \Delta C_m cos(2\pi f_m t)$ will modulate the frequency of oscillation, f_{osc}, as

$$f_c = \frac{1}{2\pi\sqrt{LC_m(t)}} = \frac{1}{2\pi\sqrt{C_m L}}\left(1 - \frac{\Delta C_m}{C_m}cos(2\pi f_m t)\right)^{\frac{-1}{2}} \tag{15}$$

As the changes of the capacitance are small, we can write for the frequency of oscillation

$$f_c = \frac{1}{2\pi\sqrt{C_m L}}\left(1 + \frac{\Delta C_m}{2C_m}cos(2\pi f_m t)\right) = f_0 + k_f cos(2\pi f_m t) = f_0 + k_f m(t) \tag{16}$$

where

$$k_f = \frac{f_0 \Delta C_m}{2C_m} \tag{17}$$

is a frequency sensitivity of the modulator with a dimension of $\frac{Hz}{Pa}$.

So the oscillator will produce a frequency modulated (FM) signal $V_s(t)$ carrying the modulating sound wave given by

$$V_s(t) = A_c cos\left(2\pi f_0 t + 2\pi k_f \int_0^t m(t)dt\right) = A_c cos\left(2\pi f_0 t + \frac{k_f}{f_m}sin(2\pi f_m t)\right) \tag{18}$$

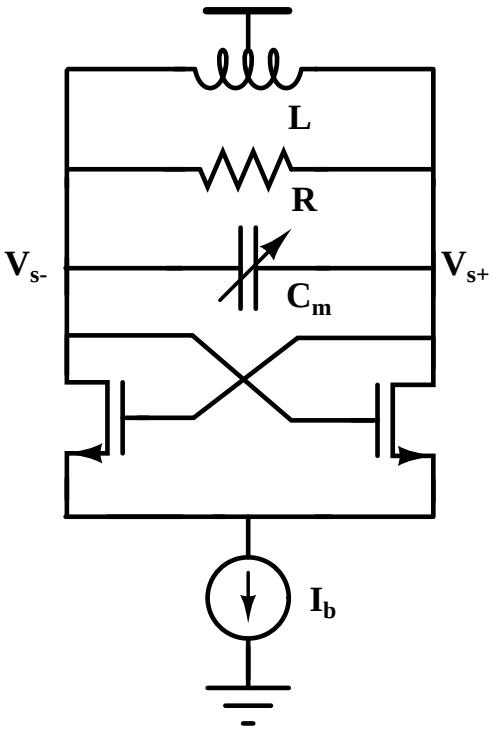

Figure 12: FM modulation of a microphone signal using an LC tank CMOS oscillator.

The FM modulated signal can be demodulated i.e. the original microphone signal recovered by using a demodulator. FM demodulation can be done in several ways for example by using a frequency discriminator or by using a PLL (phase-locked loop) [54]-[55].

Some standard large size audio equipment microphones are based on the principle of having a condenser as part of a resonating circuit. FM systems are also shown to make the speech more accessible to persons with a hearing impairment; when a speaker talks into a transmitter that FM modulates a sound signal, which is broadcasted to the listener's receiver, the strength and clarity of the signal received by the listener with a hearing impairment is enhanced because the FM system filters out the background noise [56]. Depending on the specifications based on application and purpose of an FM modulated microphone, several aspects have to be considered. We will describe some of them in a first order analysis.

From a basic telecommunication theory a frequency modulation index is defined as the ratio of the maximum frequency deviation (Δk_f) and the modulation frequency f_m, i.e. $\beta = \frac{\Delta k_f}{f_m}$ [54]. This number tells us about how many side-frequencies can be found in the spectrum of the FM signal. Therefore a rule exists about the required bandwidth for a transmission of FM waves (a sufficient number of side-frequencies should be transmitted) and it is called Carlson's rule. According to it the transmission bandwidth is $B = 2\Delta k_f(1 + \frac{1}{\beta})$. In some countries, the maximum value of frequency deviation is fixed to $75kHz$ for a commercial broadcasting by radio. With f_m for an audio signal of 15kHz, this gives $\beta = 5$ and B=180kHz.

As

$$\beta = \frac{\Delta k_f}{f_m} = \frac{f_0 \Delta C_{m,max}}{2 C_{m0} f_m} \tag{19}$$

the oscillation frequency f_0 is determined by the requirement for β and can be calculated for our case knowing that the peak $\Delta C_{m,max}$ for 20Pa sound pressure level is $20 \times \Delta C_m \times \sqrt{2} = 20 \times 2.2 \cdot 10^{-15} \frac{mV_{rms}}{Pa} \times \sqrt{2}$; with $C_m = 5.6pF$ this gives f_0=13.5MHz.

Further more, the telecommunication theory applied to a discriminator type FM receiver [54] says that in the case of a high carrier-to-noise ratio (average carrier power divided by average noise power in bandwidth of the modulated wave at the receiver input), the signal-to-noise ratio at the output is $SNR_{out} = \frac{3}{2}\beta^2 SNR_{ch}$, where SNR_{ch} is the signal-to-noise ratio of the channel between the modulator (transmitter) and the demodulator (receiver).

These figures of merit have to be taken into consideration in the non-trivial analysis of the choices of building blocks of an FM system. Leaving the noise issues of the PLL and demodulation problems aside, we will start the analysis by discussing design issues of an oscillator for our microphone.

Several attempts to integrate different types of capacitive sensors in an RC or ring oscillator circuit with an FM output can be found in literature [57]-[61] and there is research ongoing about making resonant circuits (RLC circuits) using MEMS technology [62]-[65]. An idea for having a capacitive microphone in an LC tank differential MOS oscillator is registered in [66] and a resonator circuit in an LC tank is proposed in [67]. In [57] a MEMS microphone has been integrated with a CMOS RC-type oscillator.

3.3.1 FM Modulation using an LC Tank Oscillator

An LC type oscillator is shown in Fig. 12 and its frequency of oscillation f_0 is given by (16). Choosing the oscillation frequency of 13.5MHz, for the calculated $\beta = 5$, we can calculate that with a $5.6pF$ microphone capacitor, the inductance should be 248nH which is an unacceptably high value for integration. We will continue the analysis assuming that a high frequency oscillator in a technology available was used similar to GHz examples from [68]-[69] and return to the 13.5MHz example afterwards.

The phase noise of an oscillator circuits is a widely studied phenomenon [70]-[73]. The phase noise in the $1/f^2$ region due to the transistor thermal noise ($i_D^2 = 4kT\gamma g_m \Delta f$) of the oscillator from Fig. 12 is calculated in [68] as

$$L(\Delta f) = 10 \cdot log\left(\frac{kT(\gamma+1)}{4A_c^2 C_m^2 R 4\pi^2 \Delta f^2}\right) \tag{20}$$

where k is Boltzmann constant, T temperature, γ channel thermal noise factor, C_m microphone capacitance, R tank resistor, Δf offset from the resonant frequency and A_c oscillator amplitude $A_c = \frac{I_b R}{\pi}$ with I_b oscillator bias current.

The SNR of the frequency modulated microphone can be calculated in the following way. Differentiating (18) one obtains

$$\frac{dV_s(t)}{dt} = -A_c sin\left(2\pi f_0 t + 2\pi k_f \int_0^t m(t)dt\right) \cdot (2\pi f_0 + 2\pi k_f m(t)) \tag{21}$$

The detected signal from the microphone is then

$$sig(t) = 2\pi k_f m(t) \tag{22}$$

The noise of the oscillator is calculated without the microphone signal; with phase noise $\varphi(t)$ we have

$$V_s(t) = A_c cos\left(2\pi f_0 t + \varphi(t)\right) \tag{23}$$

$$\frac{dV_s(t)}{dt} = -A_c sin\left(2\pi f_0 t + \varphi(t)\right) \cdot \left(2\pi f_0 + \frac{d\varphi(t)}{dt}\right) \tag{24}$$

and

$$noise(t) = \frac{d\varphi(t)}{dt} \tag{25}$$

However

$$\varphi(t) \Leftrightarrow 2L(\Delta\varpi) \quad and \quad \frac{d\varphi(t)}{dt} \Leftrightarrow 2(\Delta\varpi)^2 L(\Delta\varpi) \tag{26}$$

Noise power is then calculated as

$$P_{noise} = 2\int_{\Delta f_{min}}^{\Delta f_{max}} (\Delta\varpi)^2 L(\Delta\varpi)\Delta f \tag{27}$$

which is for phase noise in the $1/f^2$ region, $L(\Delta\varpi) = \frac{\alpha}{(\Delta\varpi)^2}$

$$P_{noise} = 2\int_{\Delta f_{min}}^{\Delta f_{max}} \alpha\Delta f \approx 2\alpha f_m \tag{28}$$

where f_m is the maximum frequency in m(t). The SNR of an FM modulated microphone is from previous

$$SNR = \frac{2\pi k_{f_{rms}}}{\sqrt{2f_m\alpha}} \tag{29}$$

Than using (20), the SNR of a microphone FM modulated in an LC oscillator is

$$SNR = \frac{2\pi\frac{f_o\Delta C_m}{2C_m}}{\sqrt{2f_m\frac{kT(\gamma+1)}{4A_c^2C_m^2R}}} \tag{30}$$

or alternatively written as

$$SNR = \frac{\frac{\Delta C_m}{2f_mC_m}}{\sqrt{\frac{2kT(\gamma+1)}{4A_c^2C_mQf_02\pi f_m}}} \tag{31}$$

where Q is the quality factor of the oscillator.

We can now calculate the SNR with the following data $\Delta C_m = \frac{2.3fF}{Pa}$, $C_m = 5.6pF$, $f_m = 15kHz$, transistor working in saturation with $\gamma = \frac{2}{3}$. For the oscillator parameters we choose 2GHz oscillating frequency ($L = 10^{-9}H$), Q=10 and $I_B = 1mA$, this will give 60.7dB SNR. If we increase the current to $I_B = 4mA$, we will get an SNR of 72.8dB. The calculated value is without the tail current noise and assuming that the phase noise spectrum is in the $1/f^2$ region; in $1/f^3$ region, the noise will be greater and is not taken into account in this first order analysis. Similarly for oscillations at 13.5MHz and with a non-integrated inductor of 248nH, with $I_B = 500\mu A$, the SNR will be 76dB.

Two other commonly used types of oscillators are ring and relaxation. Oscillation frequency of a ring oscillator is inversely proportional to the sum of delays from each invertor building the oscillator and modulating the load capacitance of one of the invertors would give low sensitivity of the microphone signal modulation besides the known poor phase-noise performance of ring oscillators comparing to LC tank oscillators [71], [74]. We will therefore skip the analysis of ring oscillators and look at a relaxation oscillator.

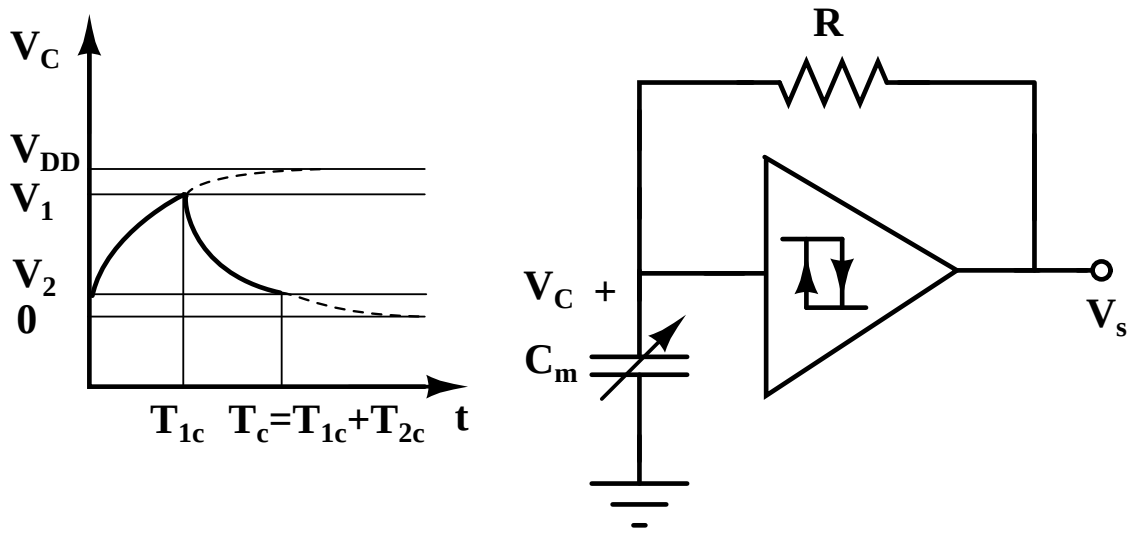

Figure 13: FM modulation of a microphone signal using a relaxation oscillator.

3.3.2 FM Modulation using an RC Oscillator

A typical relaxation oscillator with its respective waveforms is shown in Fig. 13 and its behavior and noise analysis are explained in [74]. The oscillator is composed of a Schmitt comparator in an RC feedback loop. While LC oscillators are lossless in RC oscillators the resistor noise poses a limit to the minimum achievable phase noise. Operation of the oscillator from Fig. 13 is explained as: during the first half of the period, the capacitor voltage changes exponentially from V_1 to V_2 which are the two comparison levels. The duration of the first half of the period is $T_{1c} = 2\pi RC_m(t) \cdot ln\left(\frac{V_{DD}-V_1}{V_{DD}-V_2}\right)$. Similarly, the duration of the second half of the period is $T_{2c} = 2\pi RC_m(t) \cdot ln\left(\frac{V_2}{V_1}\right)$ and the frequency of oscillation is

$$f_c = \frac{1}{T_c} = \frac{1}{T_{1c}+T_{2c}} = \frac{1}{2\pi RC_m(t) \cdot ln\left(\frac{V_{DD}-V_1}{V_{DD}-V_2} \cdot \frac{V_2}{V_1}\right)} \tag{32}$$

With a variable microphone capacitance we can calculate the FM microphone sensitivity from

$$f_c = \frac{1}{2\pi R \cdot ln\left(\frac{V_{DD}-V_1}{V_{DD}-V_2} \cdot \frac{V_2}{V_1}\right) C_m(1-\frac{\Delta C_m}{C_m}cos(2\pi f_m t))} = f_0 + k_f cos(2\pi f_m t) = f_0 + k_f m(t) \tag{33}$$

to be

$$k_f = f_0 \frac{\Delta C_m}{C_m} \tag{34}$$

Hz per Pascal, where f_0 is the oscillation frequency with the nominal microphone capacitance (no sound pressure applied).

Further more, assuming that the only noisy element of the RC oscillator is the resistor R, in [74] the phase noise in the $1/f^2$ region of a relaxation oscillator is calculated as

$$L(\Delta f) = 10 \cdot log\left(\frac{kT}{4\pi C_m V_{DD}^2}\left(\frac{1-2V_{1n}}{V_{1n}^2 ln^2(\frac{1}{V_{1n}}-1)(1-V_{1n})^2}\right)\frac{f_0}{\Delta f^2}\right) \tag{35}$$

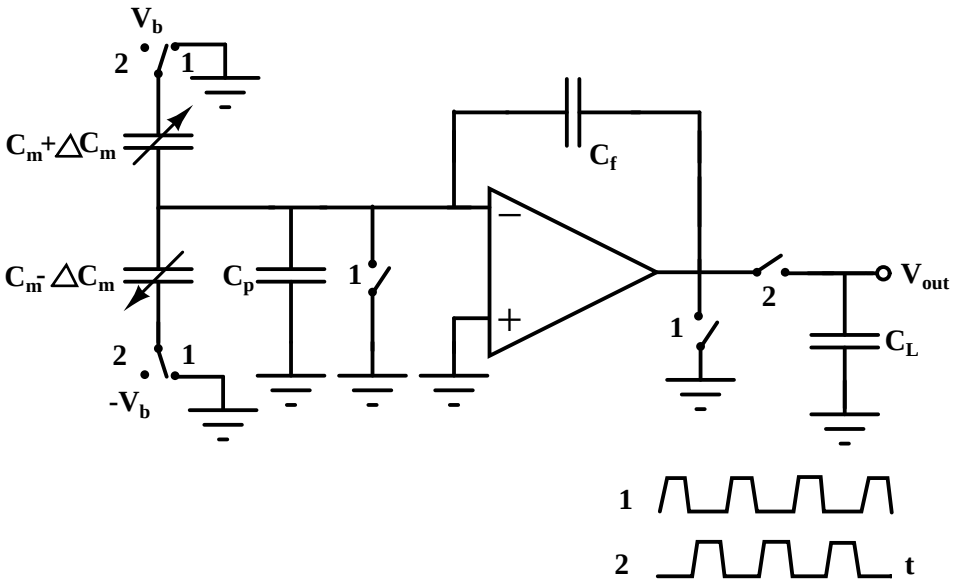

Figure 14: A switched capacitor interface to a capacitive sensor.

where V_{1n} is the normalized comparison voltage $V_{1n} = \frac{V_1}{V_{DD}}$ and $V_2 = V_{DD} - V_1$. It has been shown in the same work that the phase noise is minimal for $V_{1n} \approx 0.24$ and equals

$$L(\Delta f) = 10 \cdot log\left(\frac{5.9 f_0 kT}{C_m V_{DD}^2 2\pi \Delta f^2}\right) \tag{36}$$

We can than calculate the maximum signal-to-noise ratio that can be achieved using an RC oscillator in the same way as for the LC oscillator to be

$$SNR = \frac{\frac{f_0 \Delta C_m}{C_m f_m}}{\sqrt{\frac{2 \cdot 5.9 f_0 kT}{C_m V_{DD}^2 2\pi f_m}}} \tag{37}$$

Choosing $f_0 = 13.5MHz$, $V_{DD} = 1.8V$ and the rest as earlier, we obtain an SNR of 55dB (R is 916Ω). With the frequency of oscillation 1GHz SNR is 74dB (R is 12Ω).

3.4 Switched Capacitor Interface to Capacitive Microphone and Dynamic Offset Cancelation (DOC) Techniques

Switched capacitor (SC) circuits are well suited for use in connection with digital circuits, because they work with sampled signals they can be easily combined with A/D convertors and digital signal processing circuits. For an example of a switched capacitor amplifier refer to [38]. In some applications (MEMS accelerometer, angle detector etc.) capacitive sensors have been interfaced by using a switched capacitor charge amplifier [75]-[76]. As switched capacitor circuits rely on quickly transferring charge from one capacitor to another, it is clear that the interface to the capacitive microphone in this context should be considered when the microphone is operated in its charge sensing mode. Sampling on the high impedance nodes in the voltage sensing mode would be unpractical.

A switched capacitor interface to capacitive sensor is shown in Fig. 14. The two capacitances are shown in the figure $C_{m1} = C_m + \Delta C_m$ and $C_{m2} = C_m - \Delta C_m$ which are switched to voltages V_b and

$-V_b$. The switches in the figure are used to reset the charges in phase 1. During the phase 2 the output voltage becomes

$$V_{out} = -\frac{C_{m1} - C_{m2}}{C_f} V_b = -\frac{2\Delta C_m}{C_f} V_b \tag{38}$$

Remembering that $C_{m1,2}$ consist of a fixed capacitance and a variable capacitance, we can see that the fixed capacitances cancel out and only the small signal differential capacitance change is amplified. This would not be the case if only one sensor was used without the negatively biased C_{m2}. Comparing to the previously explained continuous time charge amplifier approach which processes only a minute portion of charge, the SC techniques amplify the entire charge on the sensing capacitor, which is the reason why switched cap interface is used in connection with differential sensors.

Examples exist of MEMS microphones with two membranes, working differentially [77]-[78], however, they are not in a commercial use due to the high cost of the MEMS process required.

The output referred noise PSD of the switched cap charge amplifier is the same as for the continuous time charge amplifier with the same topology, and as explained in [79], the PSD of the noise sampled with frequency f_s onto C_m equal

$$V_{n,C_m}^2 = \frac{kT}{C_m} \cdot \frac{2}{f_s} \tag{39}$$

dominates the input referred noise of the electronic circuit, and as the signal is not larger than with a continuous time approach with the same sensor, a SC implementation doesn't lead to any improvements. Therefore when using SC circuits, CDS (correlated double sampling or auto-zeroing) [80]-[81] is used to reduce DC offset and low frequency noise.

When using correlated double sampling, the schematics in Fig. 14 is sightly modified, an additional clock phase is added (refer to [76]); at the end of the reset phase, 1 is open and the charge and KT/C noise is injected onto the summing node, during the error sensing phase, the error is amplified and stored onto a storage capacitor, during the signal sensing phase, the sense voltages are applied to the sense capacitors; the amplifier output which contains both the signal and the error is subtracted by the error previously stored on the load capacitor and the output voltage contains the signal only.

Other complications with SC circuits are noise-folding, clock feed-through and charge sharing and it is known that although correlated double sampling (CDS) has been used to significantly reduce the noise, the noise folding and the switch noise still lead to higher noise in an SC sensing circuit than in a continuous-time sensing circuit at the same power dissipation [82].

Assuming that the flicker noise and the sampled noise are eliminated by CDS, and that the switches are ideal so that their leakage currents don't disturb an immediate charge transfer, non of which is the case in praxis, the highest SNR that can be achieved using the preamplifier from Fig. 14 would be the same as for the continuous time solution from Fig. 11. To recall, we calculated 51dB in that case with thermal noise only. So using SC techniques the SNR will never be larger than this and additionally a differential sensor is needed. More accurately, a switched capacitor circuit noise addressed in [53] can be calculated by using examples from [83].

By using CDS there is some residual noise and offset and for applications requiring a high precision, where noise or offset performance is paramount (smart sensors, biomedical amplifiers and similar) a chopping technique is used [80]-[81]. By using chopping, a signal is modulated, amplified and then

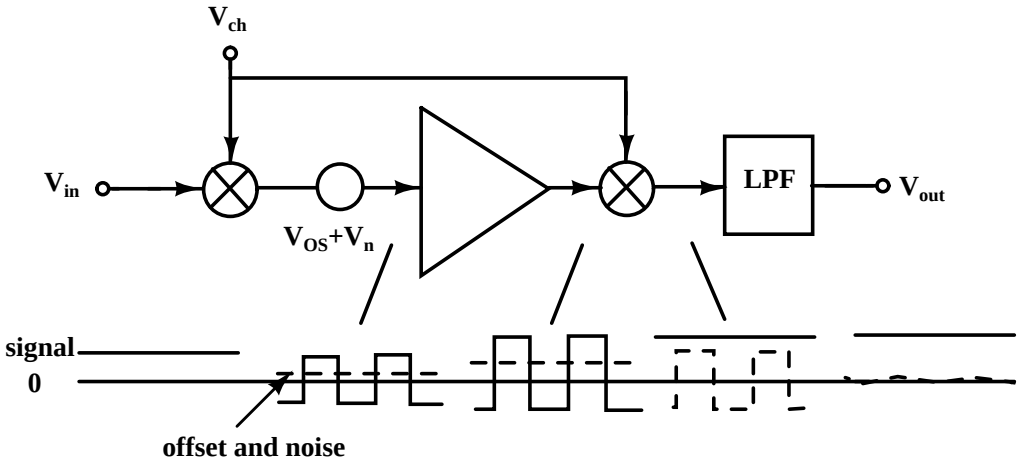

Figure 15: Chopper modulation principle.

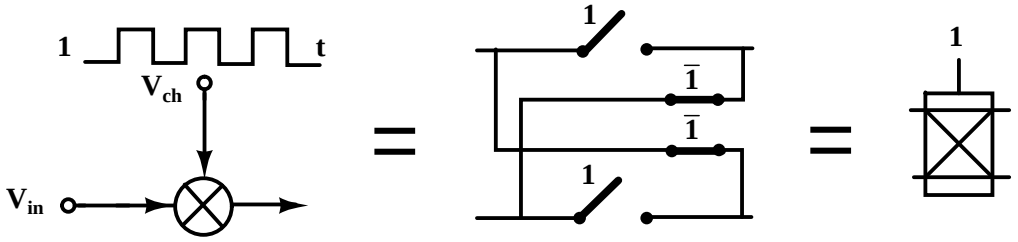

Figure 16: Switch for square-wave chopper modulation.

demodulated (Fig. 15). A low-pass filter is needed at the output. In this way, the signal is transposed to a higher frequency where there is no $1/f$ noise, amplified, and then demodulated back to the baseband. Using this technique, the noise and the offset are modulated only once and in the ideal situation, the output signal is left without any offset and low-frequency noise. Comparing to the CDS which is a sampled data technique and therefore convenient for sampled-data systems, the output signal when using chopper modulation is continuously available. Signal modulation in chopper amplifiers is done by using a polarity reversing switches as shown in Fig. 16.

In [82], [84] capacitive sensor interfaces using chopper modulation are explained. In [84] the chopping switches are connected directly to the sensor capacitor and the signal is amplified by the following SC amplifier while in some other works the multiplication is done after a bandpass amplifier interfacing the sensor. In general chopper modulation increases a circuit current consumption. The capacitive sensor interface examples from the literature using SC with CDS and chopper modulation have a rather low bandwidth. It is also possible to auto-zero a signal after chopper modulation and to do nested chopping for enhanced performance which is done in nowadays high performance opamps [80].

As explained, switched capacitor circuits (SC) sensing, CDS and chopper stabilization techniques use switches connected directly to a sensor and it is well known that non-ideal switches, most often realized using MOS transistors, produce unwanted effects such as clock feedthrough, channel charge

injection, sampled noise and leakage current.

As we have explained, in the continuous time voltage sensing mode of the capacitive microphone a very high impedance node between the microphone and the amplifier is extremely sensitive to any leakage currents and parasitic capacitances and having a switch connected to that node would hardly lead to any performance improvement. The floating gate node in the time continuous charge sensing principle is very sensitive to any disturbances as well and has to bee kept constant at any time as explained, therefore connecting a switch to the microphone is not possible either. However in both cases, switching is possible at the microphone preamplifier output and if needed noise and offset of the second stage can be minimized by DOC techniques and further processing done in the time discrete domain using SC circuits if wanted.

As explained, using switched capacitor capacitance sensing would unlikely lead to improved performance comparing to a continuous time solution (even when using CDS, noise reduction technique suitable for SC circuits) and it is left to try if a SC circuit would be functional at all in the band of interests with the microphone parasitics included and with the the non-ideal switching effects.

3.5 Sensing Methods Summary

In this section we have presented possible methods of interfacing a capacitive microphone. All nowadays miniature ECM and MEMS microphone products use a voltage sensing principle. The classical method of voltage sensing has as a drawback that a very high impedance has to be realized on chip and the settling time of these circuits may be relatively long. Further more, for MEMS microphones in the voltage sensing mode, a high bias voltage has to be generated on-chip and a high impedance isolation is needed between the biasing circuitry and the microphone. This increases the settling time as well. Distortion issues should be considered as well in implementations of amplifiers with voltage sensing because of use of non-linear bias elements. Knowing our technology noise limits, we have calculated that the maximum achievable SNR using voltage sensing would be around 63dB. As a comparison, nowadays MEMS microphone products on the market (from datasheets in the literature) have an SNR of 57dB-62dB.

Other methods of sensing a microphone have been investigated as well. It has been shown that using charge sensing will not lead to performance improvements regarding the signal-to-noise ratio (SNR) of a microphone amplifier, which is the most important parameter. Other complications with the charge sensing is that a method to keep the voltage on the microphone constant should be implemented and a solution to do it in a robust way has to be found. In the example from the literature shown an interesting floating gate technique has been implemented with a MEMS microphone, which however does not seem to be suitable for a reliable operation of a product. Biasing of the microphone is needed in this method as well and a bias voltage with a low output impedance is needed.

The method of capacitance sensing has been explained. Some studio equipment microphones which are based on the FM modulating approach exist, but those are probably not integrated solutions. We analyzed if some improvements when using our MEMS microphones can be achieved in an FM oscillating system disregarding all the non-ideal effects and assuming that the demodulation is noise-

free. In practice, if our MEMS microphone was assembled with an oscillator, the quality factor of that oscillator would be very low due to the parasitics of the sensor. Besides that, depending on the oscillation frequency required for the subsequent signal processing, for MHz frequencies it would not be possible to make an integrated solution with an LC oscillator as the size of a coil inductance is limited. With a typical GHz LC oscillator, the SNR of the FM microphone would be around 60 dB with current consumption around mA, which is already unacceptably high current consumption. Additionally, demodulation blocks are usually power hungry. Using an RC oscillator, it would be possible to achieve an SNR of 55dB with MHz oscillation frequency. An advantage of using capacitive sensing over the other approaches is that a high bias voltage is not needed. Another is that the complications of using extremely high nonlinear devices for biasing are avoided; as the high resistances are not needed, the settling time would not be an issue.

For the sake of completeness we have looked at the switched-capacitor implementation of the microphone interface, assuming that the connecting switches to the microphone would not degrade its performance and that a differential microphone required is available. The SNR which is possible to achieve with an SC circuit can in the the best case, when its ficker noise is removed by CDS be equal to the continuous time charge amplifier with thermal noise only; this is again much lower than with a voltage sensing solution.

Correlated double sampling and chopper stabilization are normally used for noise critical applications to reduce flicker noise. Both techniques can be used after the microphone preamplifier, to reduce the noise of the following circuit. Connecting a chopper switch to the microphone, would degrade its performance as well as connecting a switch for sampling to the high impedance node between the sensor and the microphone.

This analysis leads to a conclusion that the most commonly used approach i.e. voltage sensing of the capacitive microphone is still the best solution allowing a robust operation and the highest signal-to-noise ratio for an acceptable current consumption. Each of the other investigated methods has drawbacks which are at the moment unacceptable for a product in operation with the microphone as it is. The state-of-the art SNR for MEMS microphones is 57dB-62dB and is obtained in the products with voltage sensing which are currently on the market. No works have been found in the literature which would give a better result (with typical characteristics of nowadays MEMS dies) with an acceptable degradation of other properties.

4 Conclusion I

In this part we have given an introduction of condenser microphones. We revealed that a continuing minimization of condenser microphones and the advent of miniature capacitive MEMS microphones with an increased noise, calls for improved amplifier circuits with a better noise performance comparing to the existing solutions. We have investigated possible methods of amplifying a microphone signal. Due to the increased noise of nowadays small microphones, the signal-to-noise ratio of the microphone with the amplifier is the key figure of merit and has been calculated for different amplification methods. We have seen that a traditional voltage sensing solution is the most feasible approach. We point out

that nowadays microphone designs on the market with an SNR of around 60dB are very close to the limits of the technology; typically both MEMS die is optimized for having a minimum size with a minimum acceptable level of noise and the noise of CMOS electronic is close to the limits of the technology. The latest issue will be investigated in details in the following chapters of this thesis. No works have been found in the literature that reveal methods to increase the SNR higher than that of the state-of-the-art microphone products.

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5 $1/f$ Noise

Microphones are transducers that convert sound pressure into an electrical signal. Due to various physical mechanisms, spontaneous signal fluctuations, called noise, are generated in microphones. These fluctuations, observed when dealing with any type of small signals, set the minimum signal level that is possible to measure or process. Microphone signal is usually amplified by some electronic circuitry. The interfacing circuitry has own electrical noise that contributes to the noise of the entire system (microphone and preamplifier) and has to be designed for achieving optimal system noise performance, i.e. maximal signal-to-noise ratio.

To design a CMOS preamplifier with a minimal noise contribution, understanding of MOS transistor noise and accurate noise modelling is required. Two main noise sources exist from the MOS transistor channel: thermal and $1/f$ or flicker noise. As the power spectral density (PSD) of the flicker noise is inversely proportional to frequency, this type of noise dominates at low frequencies (below corner frequency, the frequency at which thermal and flicker noise have equal contributions). In modern deep submicron technologies with typical corner frequencies of tens of megahertz, noise of audio frequency analog circuits is dominated by $1/f$ noise. With the continuous trend of downscaling transistor dimensions driven by digital design, low frequency noise (inversely proportional to the transistor area) increases thus becoming a major analog design issue. In addition, novel processing steps introduced with technology downscaling lead to unpredictable deviations of strongly technology dependant $1/f$ noise [1].

Circuit techniques exist that reduce the $1/f$ noise and these are chopper stabilization and correlated double sampling [2]. It is also possible to maximize transistor area, but this leads to a higher capacitance resulting in a need for a higher current and a higher trasconductance in order to achieve the same characteristic frequency.

As understanding of a physical noise mechanism and its relations to the process and design parameters create a foundation for an optimal low-noise circuit design, in this chapter theories explaining MOS transistor $1/f$ noise origin will be revisited. Our experimental data will be analyzed based on these theories and compared to simulations using two models (SPICE and BSIM) implemented in commercially available circuit simulators.

5.1 MOS Transistor $1/f$ Noise Theory

$1/f$ noise of flicker noise, observed for the first time in vacuum tubes in 1925, is a phenomenon related to semiconductors as well as many other types of devices. It can be defined as fluctuation in the conductance with a power spectral density proportional to f^{γ} where $-1.5 < \gamma < -0.5$. Despite more than 30 years of research, $1/f$ noise is still a topic open to debate. In 1976 it was proved that the $1/f$ noise is due to the fluctuations of the conductivity [3]. Since the conductivity of a semiconductor is expressed by

$$\sigma = q\mu n \tag{40}$$

with n free-carrier density, q elementary charge and μ mobility, from

$$\delta\sigma = q\mu\delta n + qn\delta\mu \tag{41}$$

it can be seen that the fluctuations of the conductivity can be caused by the fluctuations of the number of carriers δn, by fluctuations of the mobility of carriers $\delta\mu$ or by both. Based on this, three theories are accepted for the explanation of the $1/f$ noise in MOSFET. The first, Hooge mobility fluctuation theory explains the origin of $1/f$ noise by the fluctuations of the mobility of carriers due to collisions with crystal lattices. The second, number fluctuations theory attributes $1/f$ noise to the fluctuations of the channel free carriers due to the random trapping and detrapping of charges in the oxide traps near Si-SiO_2 interface. These two theories are combined in the third, unified approach, based on the number fluctuations with correlated mobility fluctuations.

A great deal of theoretical and experimental work can be found on the $1/f$ noise in MOS transistors with measurement results confirming any of the three theories. In the following text we will summarize the existing work and show our experimental results.

5.1.1 Mobility Fluctuations ($\Delta\mu$, Hooge Model)

According to the mobility fluctuations ($\Delta\mu$) model, the origin of $1/f$ noise is attributed to the fluctuations of the carrier mobility. This model is called Hooge's model [4]. Hooge has shown that for the conductance fluctuations of an omhic sample applies

$$\frac{S_I(f)}{I^2} = \frac{S_V(f)}{V^2} = \frac{S_R(f)}{R^2} = \frac{S_G(f)}{G^2} = \frac{C_{1/f}}{f} \tag{42}$$

where $S_I(f)$, $S_V(f)$, $S_R(f)$, $S_G(f)$ are the noise spectral densities of the current I, voltage V, resistance R and conductance G. $C_{1/f}$ is a measure of the relative noise of the sample shown to be independent of the current and voltage. Further more, in 1969 Hooge proposed an empirical relation for the $1/f$ noise in homogeneous samples

$$\frac{S_G}{G^2} = \frac{\alpha_H}{Nf} \tag{43}$$

where N is the total number of charge carriers and α_H a dimensionless constant. The fact that α_H was a constant was surprising. Measurement results on different homogeneous metals and semiconductors have given the value of α_H of about 2×10^{-3} indicating that this type of fluctuations is a fundamental property of all materials. Later measured values of the α_H parameter were $2-3$ orders of magnitude lower than this originally proposed value.

Hooge suggested in 1972 that the conductance fluctuations are due to mobility fluctuations and he suggested that the mobility of a free charge carrier fluctuates as

$$\frac{S_\mu}{\mu^2} = \frac{\alpha_H}{f} \tag{44}$$

which for homogeneous samples with N free carriers reduces to

$$\frac{S_\mu}{\mu^2} = \frac{\alpha_H}{Nf} \tag{45}$$

under assumption that the mobilities of the free charge carriers fluctuate independently of each other. For inhomogeneous samples, the previous equations can be applied to volume elements.

In the experiments with highly doped semiconductors [3], Hooge and Vandamme have shown that the lattice scattering causes mobility noise. They proved the following relation in highly doped semiconductors where electrons are scattered at electrically charged defects in the lattice (impurity scattering exists) besides being scattered by phonons of the lattice vibrations.

$$\alpha_H \approx \alpha_l \left(\frac{\mu_{eff}}{\mu_l} \right)^2 \tag{46}$$

where $\alpha_l \approx 2 \times 10^{-3}$, μ_{eff} is total mobility obtained using Matthiessen's rule $\mu_{eff}^{-1} = \mu_l^{-1} + \mu_i^{-1}$, μ_l is the mobility if only lattice scattering was present and μ_i is the mobility if only impurity scattering was present. According to their theory, only the lattice scattering gives $1/f$ noise. The density of phonons fluctuates with $1/f$ spectrum and these phonons fluctuate independently of the electric current through the sample. The lattice scattering theory gives a solution to the problem that the spectrum is $1/f$ also for frequencies much lower than the inverse of the time that an electron stays in the sample. This refinement formula for α_H also explains the noticed result from measurement data that α_H depends on the crystalline quality of the material and is not a constant.

Ziel has shown [5] starting from the Langevin equation, that for a MOS device section of length Δx with a carrier number ΔN the drain current power spectral density S_{I_D} can be calculated as an integral along the channel with length L of noise in each segment

$$S_{I_D}(f) = \frac{1}{L^2} \int_0^L \Delta S_{I_D}(x, f)\, \Delta x dx \tag{47}$$

where

$$\Delta S_{I_D}(x, f) = \frac{I_D^2 S_{\Delta N}(f)}{\Delta N^2} \tag{48}$$

and

$$S_{\Delta N}(f) = \frac{\alpha_H \Delta N}{f} \tag{49}$$

giving

$$S_{I_D}(f) = \frac{1}{L^2} \int_0^L \frac{\alpha_H I_D^2}{f \Delta N} \Delta x dx \tag{50}$$

Plugging in the formula for the drain current,

$$I_D = q \mu_{eff} \frac{\Delta N}{\Delta x} \frac{dV(x)}{dx} \tag{51}$$

where $V(x)$ is the channel potential at a point x from the source, in (50) gives

$$S_{I_D}(f) = \frac{q \mu_{eff} \alpha_H I_D}{L^2 f} \int_0^{V_D} \frac{dV(x)}{dx} dx \tag{52}$$

resulting in

$$S_{I_D}(f) = \frac{q \mu_{eff} \alpha_H I_D V_D}{L^2 f} \tag{53}$$

which is known as Klaassen's formula for high-inversion MOSFET. V_D is the drain-source voltage.

For a transistor working in the ohmic region applies

$$I_D \approx \mu_{eff} \frac{W}{L} C_{ox} \left(V_{GS} - V_T\right) V_{DS} \tag{54}$$

where C_{ox}, W, L, V_{GS}, V_{DS} and V_T are oxide capacitance, transistor width, transistor length, gate-source, drain-source and threshold voltage respectively. Plugging (54) in (53) gives

$$S_{I_D}(f) = \frac{q\mu_{eff}^2 \alpha_H C_{ox} W \left(V_{GS} - V_T\right) V_{DS}^2}{L^3 f} \tag{55}$$

The same formula can be obtained by assuming for the number of carriers

$$N = \frac{C_{ox} \left(V_{GS} - V_T\right) WL}{q} \tag{56}$$

and plugging it together with (54) in the empiric formula

$$S_{I_D} = \frac{\alpha_H I_D^2}{fN} \tag{57}$$

Vandamme has shown [6]-[7] that the number of free carriers for a transistor working in the saturation region is reduced to 2/3 of the number of free carriers at zero drain source voltage, and that the relative drain current spectral density S_{I_D}/I_D^2 in saturation is two times the value in the ohmic region for the same gate source voltage. Assuming that in saturation

$$I_D \approx \frac{1}{2} \mu_{eff} C_{ox} \frac{W}{L} \left(V_{GS} - V_T\right)^2 \tag{58}$$

he shows that for strong inversion and saturation region

$$S_{I_D}(f) = 2 \left(\frac{S_{I_D}}{I_D^2}\right)_{ohmic} I_D^2 = \frac{2\alpha_H I_D^2}{fN} = \frac{1}{2} q\mu_{eff}^2 \frac{\alpha_H}{f} C_{ox} \frac{W}{L^3} \left(V_{GS} - V_T\right)^3 \tag{59}$$

A more complete derivation of the mobility fluctuation noise model for transistors working in the linear region was given in 2002 [8] taking into consideration that α_H is a function of electric field, not a constant. Starting from the expression for μ_{eff}

$$\mu_{eff} = \frac{\mu_0}{1 + \theta \left(V_{GS} - V_T\right)} \frac{1}{\sqrt{1 + \left(\frac{E(x)}{E_c}\right)^2}} \tag{60}$$

where μ_0 is the low-field mobility, θ mobility attenuation factor, $E(x) = dV(x)/dx$ horizontal channel field and E_c critical electric field when the carrier velocity saturates, the $\alpha_H = \alpha_0(\mu_{eff}/\mu_0)^2$ becomes

$$\alpha_H = \frac{\alpha_0}{\left(1 + \theta \left(V_{GS} - V_T\right)\right)^2} \frac{1}{1 + \left(\frac{E(x)}{E_c}\right)^2} \tag{61}$$

Similarly to (47)-(52) by substituting α_H (61), μ_{eff} (60) and I_D (51) and taking it under the integral in (50) one obtains

$$S_{I_D}(f) = \frac{\alpha_0 \mu_0 q}{fL^2} \int_0^{V_D} \frac{I_D}{\left(1 + \left(\frac{E(x)}{E_c}\right)^2\right)^{3/2} \left(1 + \theta \left(V_{GS} - V_T\right)\right)^3} dV \tag{62}$$

Then by replacing

$$E(x) = \frac{I_D}{\mu_{eff} q \frac{\Delta N}{\Delta x}} = \frac{I_D}{W \mu_{eff} C_{ox} (V_{GS} - V_T - V(x))} \tag{63}$$

in (62) and introducing a temporary variable $V_m = I_D/(WC_{ox}\mu_{eff}E_C)$, the expression for the mobility fluctuation noise power spectral density in linear region suggested is

$$S_{I_D}(f) = \frac{\alpha_0 \mu_0 q}{f L^2} \int_{V_1}^{V_2} \frac{I_D}{\left(1 + \left(\frac{V_m}{V}\right)^2\right)^{3/2} (1 + \theta V_2)^3} dV \tag{64}$$

where $V_1 = V_{GS} - V_T - V_D$ and $V_2 = V_{GS} - V_T$.

$1/f$ noise according to the mobility fluctuations model for transistors working in the subthreshold region has been recently (2001) presented in [9] with an improved method for calculating the total number of carriers under the gate. In the previous method of estimating the number of carriers Vandamme and Vandamme [10] proposed an empirical formula $N = C_{ox}WLkT/q^2$ with an explanation that the average energy of an electron in a two dimensional system, that corresponds to the thermal voltage kT/q, is kT. Based on this, they calculated the number of contributing carriers on a capacitor charged by kT/q as CkT/q^2. The new approach from [9] starts from the drain current in weak inversion given by

$$I_D = I_{D0} exp\left(\frac{q(V_{GS} - V_T)}{\eta kT}\right)\left(1 - exp\left(\frac{-qV_D}{\eta\prime kT}\right)\right) \tag{65}$$

with

$$I_{D0} = \frac{kT}{q} D \frac{W}{L} C_{ox} \tag{66}$$

and Einstein's relation $D = \mu kT/q$; η is weak inversion slope factor. Since

$$g(V(x)) = \frac{I_D}{dV(x)} dx = \frac{1}{\eta\prime} DWC_{ox} exp\left(\frac{q(V_{GS} - V_T)}{\eta kT}\right) exp\left(\frac{-qV(x)}{\eta\prime kT}\right) \tag{67}$$

and

$$g(V(x)) = \mu_{eff} q \frac{\Delta N}{\Delta x} \tag{68}$$

the number of carriers was calculated as

$$N = \int_0^L \frac{\Delta N}{\Delta x} dx = \frac{1}{2} \frac{1}{\eta\prime} \frac{1}{q} \frac{L^2}{D} I_D \frac{1 + exp\left(\frac{-qV_D}{\eta\prime kT}\right)}{1 - exp\left(\frac{-qV_D}{\eta\prime kT}\right)} \tag{69}$$

and the drain current power spectral density was given as

$$S_{I_D}(f) = \frac{\alpha_H I_D^2}{fN} = \eta\prime \frac{2q}{L_{eff}^2} \frac{\alpha_H}{f} D I_D th\left(\frac{qV_D}{2\eta\prime kT}\right) \tag{70}$$

This is in the ohmic region equivalent to (53) and for large drain voltages ($V_D \gg \eta' kT/q$) equals to

$$S_{I_D}(f) = \eta\prime 2qD^2 \frac{kT}{q} \frac{\alpha_H}{f} \frac{W}{L^3} C_{ox} exp\left(\frac{q(V_{GS} - V_T)}{\eta kT}\right) \tag{71}$$

Majority of experimental data up to date show that the $\Delta\mu$ model explains better noise in p-channel transistors than in n-channel because of the fact that observed input referred PSD in linear region for p-MOS depends on gate bias as shown by (55) what can not be explained by the ΔN model. However

	$S_{I_D}(f)$	ΔN model	$\Delta\mu$ model
W. i.	$f(I_D)$	$\frac{q^4 N_t(E_f) I_D^2}{kTWLf\gamma(C_d+C_{ox}+C_{it})^2}$	$\eta^{'} 2\mu_{eff} kT \frac{\alpha_H}{f} \frac{1}{L^2} \left(1 - exp\left(\frac{-qV_{DS}}{\eta' kT}\right)\right)^{-1} I_D$
Tri.	$f(I_D, V_{GS})$	$\frac{q^2 kTN_t(E_f)}{\gamma f} \frac{1}{C_{ox}^2 WL} \frac{I_D^2}{(V_{GS}-V_T)^2}$	$\frac{q\alpha_H}{f} \frac{1}{C_{ox}WL} \frac{I_D^2}{V_{GS}-V_T}$
	$f(V_{DS}, V_{GS})$	$\frac{q^2 \mu_{eff}^2 W}{fL^3} \frac{N_t(E_f) kTV_{DS}^2}{\gamma}$	$\frac{q\mu_{eff}^2 \alpha_H C_{OX} W (V_{GS}-V_T) V_{DS}^2}{L^3 f}$
Sat.	$f(I_D)$	$\frac{q^2 \mu_{eff}}{C_{ox} L^2} \frac{N_t(E_f) kT}{\gamma} \frac{I_D}{f}$	$q\sqrt{2} \frac{\alpha_H}{f} \frac{\sqrt{\mu_{eff}}}{\sqrt{C_{ox} WL^3}} I_D^{3/2}$
	$f(V_{GS})$	$\frac{1}{2} q^2 \mu_{eff}^2 \frac{kTN_t(E_f)}{\gamma f} \frac{W}{L^3} (V_{GS} - V_T)^2$	$\frac{1}{2} q\mu_{eff}^2 \frac{\alpha_H}{f} C_{ox} \frac{W}{L^3} (V_{GS} - V_T)^3$

Table 3: Drain current PSD according to ΔN and $\Delta\mu$ models for different operating regions.

majority of experiments show ΔN model more appropriate for explaining noise in weak inversion for both types of transistors. These observations have resulted in the origin of $1/f$ noise still being an often discussed issue.

Described noise formulas summarized for different operating regions and as a function of both V_{GS} or I_D are shown in Table 3. This table is from [11].

5.1.2 Carrier Number Fluctuations (ΔN, McWhorter Model)

McWhorter carrier number fluctuations (ΔN) model [12] explains the noise origin by the fluctuations of the number of channel free carriers due to the random trapping and detrapping of charges in the oxide traps near the Si-SiO_2 interface. According to this theory, a single trapping detrapping event causes a random telegraph signal (RTS) having a Lorentzian or a generation-recombination spectrum. In submicron technologies for transistor gate sizes less than a micrometer, an RTS signal from a single trap has even become visible.

The number of free carriers N fluctuates as they occupy a fraction of traps in a semiconductor, and the transitions between the traps and the conduction band of the trapping-detrapping process can be described by

$$-\frac{d\Delta N}{dt} = \frac{\Delta N}{\tau} \tag{72}$$

where τ is the trapping time constant. The corresponding correlation function [13]

$$\Psi_N(t) = \overline{(\Delta N)^2} exp(-t/\tau) \tag{73}$$

has the so called Lorentzian spectrum given by

$$S_N(f) = \overline{(\Delta N)^2} \frac{4\tau}{1 + (2\pi f\tau)^2} \tag{74}$$

A main difficulty in understanding $1/f$ noise is that no physical model can be found that has $1/f$ spectra and on which mathematics (72-74) can be applied to. For over half a century an accepted solution has been that the $1/f$ spectrum is obtained by summing a large number of Lorentzian spectra [13]. McWhorter applied this idea to semiconductors and the model has got his name. Mathematics explaining the origin of $1/f$ noise as a sum of Lorentzians is as follows.

If the probability $g(\tau)\, d\tau$ is normalized as

$$\int_0^\infty g(\tau)\, d\tau = 1 \tag{75}$$

and if the statistical weights of a Lorentzian spectra are proportional to τ^{-1} for relaxation times $\tau_1 < \tau < \tau_2$ as

$$g(\tau)d\tau = \frac{1}{ln\left(\tau_2/\tau_1\right)}\frac{1}{\tau}d\tau \tag{76}$$

and

$$g(\tau)d\tau = 0 \tag{77}$$

otherwise, then

$$S_N\left(f\right) = 4\overline{\Delta N^2}\int_{\tau_1}^{\tau_2}\frac{\tau g\left(\tau\right)d\tau}{1+\left(2\pi f\tau\right)^2} = \frac{2\overline{\Delta N^2}}{\pi f ln\left(\tau_2/\tau_1\right)}\left(arctan\left(2\pi f\tau_2\right) - arctan\left(2\pi f\tau_1\right)\right) \tag{78}$$

The latter formula yields the $1/f$ spectrum in the frequency range τ_2^{-1} to τ_1^{-1} since for $f < \frac{1}{2\pi\tau_2}$

$$S_N(f) = \frac{4\overline{\Delta N^2}\tau_2}{ln\left(\tau_2/\tau_1\right)} \tag{79}$$

for $\frac{1}{2\pi\tau_2} < f < \frac{1}{2\pi\tau_1}$

$$S_N(f) = \frac{\overline{\Delta N^2}}{ln\left(\tau_2/\tau_1\right)}\frac{1}{f} \tag{80}$$

and for $f > \frac{1}{2\pi\tau_1}$

$$S_N(f) = \frac{\overline{\Delta N^2}}{ln\left(\tau_2/\tau_1\right)\pi^2\tau_1}\frac{1}{f^2} \tag{81}$$

In this way, by the summation of the generation-recombination (Lorentzian) spectra the McWhorter model gives a $1/f$ spectrum in a natural way. However, because of the fact that the $1/f$ spectra are observed in a broad frequency range, the summing approach requires that the distribution of time constants $1/\tau$ holds over a large range and that the physical processes at different τ are independent. The desired distribution function $g\left(\tau\right)d\tau$ with properties (75)-(77) can be explained in several ways [5], [13]. The appropriate solution for $1/f$ noise is that the desired distribution function arises due to electrons interacting with the traps by quantum-mechanical tunneling of carriers from the Si/SiO_2 interface to traps located inside the oxide. In that sense, since the process is due to tunneling

$$\tau = \tau_1 exp(\gamma z); \qquad \tau_2 = \tau_1 exp(\gamma z_0) \tag{82}$$

$$g(\tau)d\tau = \frac{dz}{z_0}, \quad for \quad 0 < z < z_0 \quad and \quad 0 \quad otherwise \tag{83}$$

where γ is the tunneling parameter $10^8 cm^{-1}$, z is a distance from the surface and z_0 is the average distance between traps.

Even though McWhorter model has been accepted for a long time, some authors critically discuss the additivity of generation-recombination spectra in recent literature [14]-[15]. As for the mobility fluctuation model, derivations of the ΔN model formulas for the three operating regions will be shown here.

Because of the theory that electrons tunnel from traps in the oxide, fluctuations of the number of trapped electrons ΔN_t in a volume element $\Delta x\Delta y\Delta z$ have a mean square value

$$\delta\overline{\Delta N_t^2} = \Delta N_t(E)\Delta E\Delta x\Delta y\Delta z f_t(1-f_t) \tag{84}$$

$\Delta N_t(E)$ is the number of traps per unit volume with an energy between E and ΔE and f_t Fermi function $f_t = 1/(1 + exp((E - E_f)/kT))$. With the time constant τ as in (82), the corresponding spectrum is

$$S_{\Delta N_t}(f) = 4N_t(E)\Delta E\Delta x\Delta y\Delta z f_t(1 - f_t)\frac{\tau}{1 + \varpi^2\tau^2} \tag{85}$$

When integrated with respect to E, z and y this gives [5]

$$S_{\Delta N_t}(x, f) = \frac{N_t(E_f)kT}{f}\frac{W\Delta x}{\gamma} \tag{86}$$

where $N_t(E_f)$ is the trap density per unit energy at the Fermi level. Reimbold has shown [16] that the spectrum of the number of fluctuation $\delta\Delta N$ at any inversion level is

$$S_{\Delta N}(x, f) = \frac{N_t(E_f)kT}{f}\frac{W\Delta x}{\gamma}\left(\frac{\delta\Delta N}{\delta\Delta N_t}\right)^2 \tag{87}$$

with

$$\frac{\delta\Delta N}{\delta\Delta N_t} = -\frac{C_i}{C_i + C_{ox} + C_d + C_{it}} \tag{88}$$

where C_i is the channel charge capacitance, C_{ox} oxide capacitance, C_d depletion charge capacitance and C_{it} interface traps capacitance per unit area respectively. At weak inversion C_i and $N_t(E_f)/\gamma$ are independent of bias and $C_i \ll C_{ox} + C_d + C_{it}$.

Starting from the Langevin/Klaasan's theory (47)-(48), using (87)-(88) and by replacing $\Delta N = NW\Delta x$ (N is the electron density in the channel per unit area) and $C_i = q^2N/(kT)$, Ziel has shown [5] that

$$\Delta S_{I_D}(x, f) = \frac{I_D^2 S_{\Delta N}(f)}{\Delta N^2} = \frac{q^4 N_t(E_f) I_D^2}{kTW\Delta x f\gamma(C_d + C_{ox} + C_{it})^2} \tag{89}$$

and

$$S_{I_D}(f) = \frac{1}{L^2}\int_0^L \Delta S_{I_D}(x, f)\,\Delta x dx = \frac{q^4 N_t(E_f) I_D^2}{kTWLf\gamma(C_d + C_{ox} + C_{it})^2} \tag{90}$$

Similarly, in strong inversion, substituting $I_D = q\mu_{eff}(\Delta N/\Delta x)dV(x)/dx$ and (87) in (48), one obtains

$$S_{I_D}(f) = \int_0^L \frac{q^2\mu_{eff}^2 W\left(\frac{dV(x)}{dx}\right)^2}{fL^2}\frac{N_t(E_f)kT}{\gamma}\left(\frac{\delta\Delta N}{\delta\Delta N_t}\right)^2 dx \tag{91}$$

For $dV(x)/dx = V_{DS}/L$ and $(\delta\Delta N/\delta\Delta N_t)^2 = 1$ the latter formula reduces to an expression for a transistor working in the linear region

$$S_{I_D}(f) = \frac{q^2\mu_{eff}^2 W}{fL^3}\frac{N_t(E_f)kTV_{DS}^2}{\gamma} \tag{92}$$

In strong inversion in saturation

$$S_{I_D}(f) = \frac{q^2\mu_{eff}}{C_{ox}L^2}\frac{N_t(E_f)kT}{\gamma}\frac{I_D}{f} \tag{93}$$

what can be derived by the procedure (numerical solving of an integral) described by Ziel [5], by using the approach described in [17], or by using equations for linear region and modifying them based on the fact that the relative drain current spectral density S_{I_D}/I_D^2 in saturation is two times the value in the ohmic region for the same gate source voltage.

In most of the experimental data up to date drain current power spectral density of both n- and p-channel transistors in weak inversion shows quadratic dependance of drain current as given by the expression (90) supporting the number fluctuation model; for $\Delta\mu$ model, the drain current PSD in weak inversion is proportional to I_D (70). Further more, a lot of data for n-transistors show S_{I_D}/μ_{eff} with no V_{GS} dependence in linear region what can be described only by the ΔN model (92) since α_H is a constant. In addition, it is often said that p-transistors are following the $\Delta\mu$ theory as their S_{I_D}/μ_{eff} is proportional to $V_{GS} - V_T$ according to (55). This is known as the controversy about the origin of $1/f$ noise that has been discussed by scientists for over 30 years. A summary of experimental results from literature and our measurement data will be shown in the following text.

5.1.3 Unified ($\Delta N - \Delta\mu$) Models

Unified noise models [18]-[19] were derived in late eighties in an attempt to come to a universal model valid for both n- and p-channel transistors in all operating regions. These modeling efforts combine the two previously described approaches in the correlated number and mobility fluctuations model called ΔN-$\Delta\mu$ model. The unified model takes into account that the oxide/interface traps apart from modulating the number of carriers, indirectly interact with the carrier mobility through Coulombic scattering.

Starting from the ΔN theory, Ghibaudo [18] has shown that charge fluctuations due to the fluctuations of the number of carriers can be described by the fluctuations of the flatband voltage as

$$\delta V_{fb} = -\frac{\delta Q_i}{C_{ox} W L} \tag{94}$$

and that the flatband voltage spectral density takes the form

$$S_{V_{fb}} = \frac{S_{Q_i}}{C_{ox}^2 W L} \tag{95}$$

From the charge conservation equation he has also shown that the transistor gate voltage and the flatband voltage have the same power spectral density i.e. that

$$S_{I_D} = g_m^2 S_{V_g} = g_m^2 S_{V_{fb}} = g_m^2 \frac{S_{Q_i}}{C_{ox}^2 W L} \tag{96}$$

where g_m is transconductance and S_{I_D} drain current power spectral density. To account for the extra mobility fluctuation due to scattering he writes

$$\delta I_D = -g_m \delta V_{fb} \pm \alpha_s \mu_{eff} I_D \delta Q_i \tag{97}$$

where α_s is scattering parameter. The normalized drain current power spectral density for the unified model is thus

$$\frac{S_{I_D}}{I_D^2} = \left(1 + \alpha_s \mu_{eff} C_{ox} \frac{I_D}{g_m}\right)^2 \left(\frac{g_m}{I_D}\right)^2 S_{Vfb} \tag{98}$$

and the equivalent input gate voltage power spectral density is

$$S_{V_g} = \left(1 + \alpha_s \mu_{eff} C_{ox} \frac{I_D}{g_m}\right)^2 S_{Vfb} \tag{99}$$

For $\alpha_s \simeq 0$ i.e. when the mobility fluctuations are independent of the inversion charge fluctuations (96) applies. Since the flatband voltage spectral density is given by

$$S_{Vfb} = \frac{q^2 kTN_t}{\gamma WLC_{ox}^2} \frac{1}{f} \tag{100}$$

and in weak inversion

$$\frac{g_m}{I_D} \approx \frac{q}{kT} \frac{1}{\eta} \tag{101}$$

where η is weak inversion slope factor given by $(\mathrm{C}_{ox}+\mathrm{C}_d+\mathrm{C}_{it})/\mathrm{C}_{ox}$, it can be shown that

$$\frac{S_{I_D}}{I_D^2} = \frac{g_m^2}{I_D^2} S_{Vfb} = \frac{q^4 N_T}{kTWLf\gamma(C_d + C_{ox} + C_{it})^2} \tag{102}$$

which is the same as the result in (90). Similarly, by plugging in the expression

$$\mu_{eff} = \frac{\mu_0}{1 + \theta(V_{GS} - V_T)} \tag{103}$$

and

$$\frac{I_D}{g_m} = (V_{GS} - V_T)\left(1 + \theta\left(V_{GS} - V_T\right)\right) \tag{104}$$

in (99) [18], it can be shown that the input referred noise voltage density takes the form

$$S_{V_g} = (1 + \alpha_s \mu_0 C_{ox}(V_{GS} - V_T))^2 S_{V_{fb}} \tag{105}$$

where μ_0 is low field mobility and V_{GS} gate-source voltage.

As can be noticed from the formulas describing ΔN and $\Delta\mu$ models from Table 3 in the ohmic region, the number fluctuations model can not explain input voltage spectral density dependence on the gate-source voltage usually observed on the experiments with p-transistors, while that is possible by the mobility fluctuations model predicting a linear increase. This dependence can be predicted by the unified model as (105) tells us. At the same time, as shown by (102) in weak inversion the unified noise model simplifies to ΔN model which is usually appropriate for both types of transistor in this region. A form of the unified model noise expression is implemented in the widely used BSIM3v3 [19]-[21] circuit simulator model which will be presented next. The model used for BSIM3v3 has been though derived in a different way comparing to the one shown here.

At this point it is important to note that an observation of the S_{I_D}/I_D^2 and $(g_m/I_D)^2$ plots in linear region versus drain current is considered a generic procedure for determining the $1/f$ noise origin [22]. If there is a good correlation between S_{I_D}/I_D^2 variations versus drain current and the corresponding transconductance to drain current ratio squared $(g_m/I_D)^2$ versus drain current, the dominating mechanism is ΔN. A departure from the $(g_m/I_D)^2$ characteristics can be explained by (98) by the influence of additional correlated mobility fluctuation. Second diagnostic method is a plot of the input referred noise PSD as a function of gate bias.

From the theory presented so far, it can be seen that there are three physical parameters relevant for quantitative determination of $1/f$ noise. These physical parameters are oxide trap density N_t, Hooge parameter α_H and Coulomb scattering parameter α_s. They can be extracted from measurement data for different bias conditions when transistor conduction parameters and presented mathematical

relations for noise are known. The conduction parameters $\mu_0, V_T, \Delta L$ and η can be extracted from measurements as well. Parameter extraction methods will be explained in the subsection dealing with our experiments.

It is usually shown in literature that the unified model shows a satisfactory fitting to the experimental data for both p- and n-channel devices. However, critical discussions on its exactness exist. Authors in [23] show that the correlated mobility fluctuations have negligible influence if the correct dependence of the Coulomb scattering limited mobility on the the inversion carrier density has been taken into account $\alpha_s = 1/(\mu_{CO}\sqrt{N})$. They claim that the unified models can not predict $1/f$ noise unless non-physical fitting parameters are used. Some other discussions in [24] deal with the use of the flatband perturbation technique (used by Ghibaudo in his unified model derivations) opposing the claim that this method can be used in strong inversion in saturation region.

5.2 Circuit Simulator Models

Three main flicker noise mechanisms have been presented so far. Understanding of a physical noise mechanisms is necessary for a successive simulator model implementation and reliable simulators are a necessity for an optimal low-noise design. The simplest empirical models called SPICE models are traditionally implemented in circuit simulators in two forms

$$S_{I_D} = \frac{KF \cdot I_D^{AF}}{C_{ox} L^2 f^{EF}} \tag{106}$$

and

$$S_{I_D} = \frac{KF \cdot I_D^{AF}}{C_{ox} LW f^{EF}} \tag{107}$$

Referred to the input the first would reduce to a form often used for hand noise calculations

$$S_{V_g} = \frac{K}{C_{ox} LW f} \tag{108}$$

($K = KF/(2\mu C_{ox})$ and EF=1). KF and EF are flicker noise coefficient and exponent respectively. Comparing these equations with the equations summarized in Table 3 it can be easily concluded that this model is oversimplified for predicting noise in different operating regions and for all types of noise mechanisms. Only ΔN model in saturation has similar parameter dependance as (106). This noise study has been initiated as the only model our circuit design team has been provided with by the foundry used for producing devices in a low-noise 0.35μm technology was this simple model. Huge discrepancies have been observed between simulations and measurements not only due to its nonability to predict noise in all operating regions but also showing higher KF parameter value in simulations than measured.

Derivations of a widely used, BSIM [21] simulator noise model are presented in 1990 starting from the theory for integration of small segments (47)-(48) and based on the unified noise model approach that the fluctuations in the trapped oxide charge will introduce correlated fluctuations of the channel carrier number and mobility. Similarly to ΔN and $\Delta\mu$ models derivation, BSIM model is based on

[20]

$$S_{I_D}(f) = \frac{1}{L^2}\int_0^L \Delta S_{I_D}(x,f)\,\Delta x dx = \\ = \frac{kTqI_D\mu_{eff}}{\gamma f L^2}\int_0^{V_D} N_t(E_f)\left(1 \pm \alpha\mu_{eff}NR^{-1}\right)^2 \frac{R^2}{N}dV \tag{109}$$

where R is $\delta\Delta N/\delta\Delta N_t$ from (88). Then the three BSIM noise parameters: NOIA, NOIB and NOIC have been introduced as

$$N_t^*(E_f) = N_t(E_f)\left(1 \pm \alpha\mu_{eff}NR^{-1}\right)^2 \tag{110}$$

$$N_t^*(E_f) = \frac{1}{q}\left(NOIA + NOIB\cdot N + NOIC\cdot N^2\right) \tag{111}$$

where $N_t^*(E_f)$ is the equivalent oxide trap density that produces the same noise power if there were no contributions from the mobility fluctuations. Comparison with the physical noise parameters and the BSIM unified theory is done in [20]. Comparing (109) in the ohmic region with (52), a relation with BSIM and the $\Delta\mu$ model is obtained through Hooge's parameter given as

$$\alpha_H = \frac{kT}{\gamma}N_t(E_f)\left(\frac{1}{N} + 2\alpha\mu_{eff} + \alpha^2\mu_{eff}^2 N\right) \tag{112}$$

and comparing the (109) in the ohmic region with (91), a relation with BSIM and ΔN model is obtained through the following relation for the number of traps

$$N_t(E_f)_{eff} = N_t(E_f)\left(1 + \alpha\mu_{eff}N\right)^2 \tag{113}$$

The final formulation of the BSIM3v3 flicker noise model is coded in circuit simulators in strong inversion for $(V_{GS} - V_T) \geq 0.1$ as [21]

$$S_{I_D} = \frac{kTq\mu_{eff}I_D}{\gamma C_{ox}L^2 f^{EF}}\left(NOIA\cdot log\left(\frac{N_0+N^*}{N_L+N^*}\right) + NOIB\left(N_0 - N_L\right) + \frac{NOIC}{2}\left(N_0^2 - N_L^2\right)\right) \\ + \frac{kTI_D^2\Delta L_{clm}}{qWL^2 f^{EF}}\frac{NOIA + NOIB\cdot N_L + NOIC\cdot N_L^2}{\left(N_L+N^*\right)^2} \tag{114}$$

N_0 and N_L are carrier densities at the source and drain ends of the channel given by

$$N_0 = \frac{C_{ox}}{q}(V_{GS} - V_T) \tag{115}$$

$$N_L = \frac{C_{ox}}{q}\left(V_{GS} - V_T - min(V_{DS}, V_{DSat})\right) \tag{116}$$

ΔL_{clm} refers to the channel length reduction (modulation) that exists only in saturation, i.e. for a drain-source voltage greater than saturation voltage V_{DSat} and is given by

$$\Delta L_{clm} = L_{itl}\cdot log\left(\frac{\frac{V_{DS}-V_{DSat}}{L_{itl}} + E_M}{E_{SAT}}\right) \tag{117}$$

with $L_{itl} = \sqrt{\varepsilon_{si}t_{ox}X_j/\varepsilon_{ox}}$; critical field at which the carrier velocity saturates is $E_{SAT} = \frac{2V_{SAT}}{\mu_0}$, $V_{SAT} = 1.5\cdot 10^5 m/s$ and E_M is the maximum electric field equal to $4.1\cdot 10^7 Vm^{-1}$.

In weak inversion this model predicts

$$S_{I_{Dwi}} = \frac{NOIA \cdot kTI_D^2}{\gamma q W L f^{EF} N^{*2}} \tag{118}$$

where $N^* = kT/q^2(C_{ox} + C_d + C_{it})$, coded as 10^{14}. For the continuity between subthreshold and above threshold formulas the following equation is used

$$S_{I_D} = \frac{S_{I_{Dwi}} S_{lim}}{S_{I_{Dwi}} + S_{lim}} \tag{119}$$

where S_{lim} is the noise calculated using (114) at $V_{GS} = V_T + 0.1$

For $V_{DS} \ll (V_{GS} - V_T)$ and using (54) the equation (114) reduces to

$$S_{I_D} = \frac{kT\mu_{eff}^2 W}{L^3 f^{EF}} C_{ox} V_{DS}^2 \left(NOIB\,(V_{GS} - V_T) + \frac{C_{ox}}{q} NOIC\,(V_{GS} - V_T)^2 \right) \tag{120}$$

By comparing the latter formula with NOIC neglected with the $\Delta\mu$ model from (55) it is easy to show that

$$NOIB = \frac{q\alpha_H \gamma}{kT} \tag{121}$$

When comparing it with the ΔN model from (92) we obtain

$$NOIB = \frac{q^2 N_t(E_f)}{C_{ox}\,(V_{GS} - V_T)} \tag{122}$$

Equation (122) shows that for proper modeling of the ΔN noise, the parameter NOIB is voltage dependent. This is implemented in BSIM3v3 simulator model for version parameter VER=3.24. Finally by comparing formulas (118) and (90) it can be shown that NOIA parameter takes the form

$$NOIA = qN_t(E_f) \tag{123}$$

It can be noted that in some works, $NOIA = q\gamma N_t$, so a care should be taken when comparing parameter values provided by different authors. The default value for N* in (118) usually coded in simulators is 10^{14}.

The procedure for extraction of BSIM parameters is [25], [26]: NOIA is extracted from the measurement data in subthreshold, NOIB from the plot of S_{I_D}/μ_{eff}^2 versus $V_{GS} - V_T$ for low drain biases, and then NOIC is obtained from measurements at high $V_{GS} - V_T$ knowing NOIA and NOIB. Afterwards based on measurements at higher V_{DS} these parameters need to be matched.

Even though unified noise models show good fitting with experimental data, one of the questions still open is a physical understanding of the scattering parameter α_s. According to the discussions presented in [23], the correlated mobility fluctuations are negligible compared to the carrier number fluctuations. The correct expression for the $N_t^*(E_f)$ is given by

$$N_t^*(E_f) = N_t(E_f) \left(1 + \frac{\mu_{eff}\sqrt{N}}{5.9 \cdot 10^8} \right)^2 \tag{124}$$

with the only fitting parameter being $N_t(E_f)$. This is different from (110) and the good agreement between BSIM model and experimental data is explained by the use of non-physical values for the parameters NOIA, NOIB and NOIC.

Another source of $1/f$ noise is the series resistance noise due to the voltage drop on the source and drain regions near the channel. This type of access resistance noise is observed for high gate-source voltages, i.e. for increased drain currents and particularly for LDD (lightly doped drain) and MDD (medium doped drain) MOST with a reduced channel length. Methods for extraction and calculation of this type of noise are explained in for example [11]. Series resistance noise has the same bias dependance as the $\Delta N - \Delta\mu$ noise model and that model can by extracting α_s parameter from measurement data be used for predicting the noise of a device with access noise. However, BSIM model does not take series resistance noise into consideration. Access resistance noise has not been observed for relatively low bias voltages in our measurements.

Other popular circuit simulator model is the charge-based EKV transistor model [27]. Flicker noise has been in that model for long time described by a simple formula

$$S_{V_g} = 4kT\frac{\rho}{WLf} \tag{125}$$

with ρ defined as approximately being a constant with dimension $(As/m)^2$. This formulation is true in the sense that all existing noise mechanisms predict input referred noise which is inversely proportional to the transistor area, however dependence of ρ on bias, process and temperature is usually much greater than what allows one to call it a constant. In the new literature (2006) on the EKV model [28], complete noise formulas have been derived starting from the ΔN and $\Delta\mu$ theories and using the physical parameters described in these models along with the usual EKV model parameters used to describe MOS transistor operation. These new model equations were not available in the beginning of this noise study (2005). Due to the fact that they are valid in all regions of operation they will be used for noise optimization of an amplifier with a capacitive source described in the next part of this thesis.

5.3 Technology Scaling and Processing Steps Influence

It is well known that with decreasing transistor dimensions, $1/f$ noise increases. Besides that, noise is strongly technology dependent and new technological processes accompanying device scaling lead to sometimes unpredictable noise behavior. In average, noise is increased with technology scaling and also noise variations from die to die and sample to sample are increased in smaller devices. With technology scaling oxide thickness decreases and to minimize short channel effects and obtain lower threshold voltages some extra processing steps need to be introduced. An example of a processing step to optimize short-channel effect is to use BF_2 (instead of B) implantation, but to avoid boron penetration through the oxide in the presence of fluorine, an additional step nitridation of the oxide is needed. In return, using nitridation increases $1/f$ noise as shown by several authors [1], [29]-[31]. Actually, it has been shown that the number of traps N_t increases for any type of nitridation process chemical formula. Nitridation is usually introduced after oxidation for transistor dimensions less than $0.35\mu m$.

Ref.	Tech.	n/p	Origin	N_t $(eV^{-1}cm^{-3})$	α_H	$\alpha_s(Vs/C)$	$t_{ox}(nm)$
[9]	0.8μ	p	$\Delta\mu$ wi, si		$1.3 \cdot 10^{-5}$		
[11]	0.09μ	p	ΔN wi, $\Delta\mu$ si	$3 \cdot 10^{17}$	$3.6 \cdot 10^{-4}$	$1.4 \cdot 10^{5}$	1.5
[16]		n	ΔN wi, si	$3 \cdot 10^{16}$			120
[19]		n	ΔN wi, si	$6 \cdot 10^{16}$			50
[19]		n	ΔN wi, si	$5 \cdot 10^{16}$			10.3
[23]	0.25μ	p	ΔN wi, $\Delta\mu$ si	$5 \cdot 10^{16}$		$2 \cdot 10^{4}$	4.9
[25]	0.8μ	n	ΔN wi, si				16
[25]	0.8μ	p	ΔN wi, $\Delta\mu$ si				16
[31]	0.13μ	n	ΔN wi, si	$8.25 \cdot 10^{16}$	$7.22 \cdot 10^{-5}$	$4.97 \cdot 10^{3}$	2.82
[31]	0.18μ	n	ΔN wi, si	$7.91 \cdot 10^{16}$	$4.06 \cdot 10^{-5}$	$6.97 \cdot 10^{2}$	3.9
[31]	0.25μ	n	ΔN wi, si	$1.84 \cdot 10^{16}$	$1.7 \cdot 10^{-5}$	$1.42 \cdot 10^{3}$	6.1
[31]	0.35μ	n	ΔN wi, si	$8.41 \cdot 10^{15}$	$3.41 \cdot 10^{-6}$	$9.68 \cdot 10^{3}$	7.65
[31]	0.13μ TG	n	ΔN wi, si	$2.11 \cdot 10^{16}$	$2.4 \cdot 10^{-5}$	$4.97 \cdot 10^{3}$	7.08
[31]	0.18μ TG	n	ΔN wi, si	$6.36 \cdot 10^{16}$	$7.59 \cdot 10^{-5}$	$4.97 \cdot 10^{3}$	7.4
[31]	0.25μ TG	n	ΔN wi, si	$5.82 \cdot 10^{16}$	$6.45 \cdot 10^{-5}$	$4.97 \cdot 10^{3}$	7.9
[32]		n	ΔN wi, si	$1.8 \cdot 10^{15}$	$2.9 \cdot 10^{-6}$		30
[32]		n	ΔN wi, si	$1 \cdot 10^{15}$	$2.1 \cdot 10^{-6}$		77
[32]		p	$\Delta\mu$ wi, si	$2.4 \cdot 10^{15}$	$1.9 \cdot 10^{-6}$		44
[32]		p	$\Delta\mu$ wi, si	$2.5 \cdot 10^{15}$	$7.1 \cdot 10^{-6}$		70
[33]	0.18μ	n	ΔN wi, si	$2.7 \cdot 10^{17}$		$4.7 \cdot 10^{3}$	3.5
[34]	0.25μ	p	ΔN wi, $\Delta\mu$ si	$2.8 \cdot 10^{16}$	$5 \cdot 10^{-5}$	$1.5 \cdot 10^{5}$	6
[34]	0.18μ	p	ΔN wi, $\Delta\mu$ si	$3 \cdot 10^{17}$	$2 \cdot 10^{-4}$	$2.3 \cdot 10^{5}$	3.5
[34]	0.13μ	p	ΔN wi, $\Delta\mu$ si	$5.6 \cdot 10^{17}$	$7 \cdot 10^{-4}$	$1.3 \cdot 10^{5}$	2
[35]	0.045μ	n	ΔN wi, si	$3.5 \cdot 10^{17}$			1.5
[35]	0.035μ	n	ΔN wi, si	$4.5 \cdot 10^{17}$			1.2
[36]	0.25μ	n	ΔN wi, $\Delta\mu$ si	$1.56 \cdot 10^{18}$	$7 \cdot 10^{-6}$		6
[37]	0.18μ	n	ΔN wi, si	$2.3 \cdot 10^{17}$		$2.8 \cdot 10^{3}$	4.5
[37]	0.18μ	p	ΔN wi, $\Delta\mu$ si	$2.3 \cdot 10^{17}$		$5.5 \cdot 10^{4}$	4.5
[38]	0.5μ	n	ΔN wi, si	$7.69 \cdot 10^{14}$			11.5
[38]	0.5μ	p	ΔN wi, $\Delta\mu$ si	$1.53 \cdot 10^{14}$			11.5
[38]	2μ	n	ΔN wi, si	$7.7 \cdot 10^{16}$			40
[38]	2μ	p	ΔN wi, si	$1.53 \cdot 10^{15}$			40
[39]	0.18μ	p	ΔN wi, $\Delta\mu$ si	$1.5 \cdot 10^{17}$		$2 \cdot 10^{4}$	4
Our data	0.13μ	n	ΔN wi, si	$4 \cdot 10^{17}$			2.4
Our data	0.13μ	p	ΔN wi, $\Delta\mu$ si	$4 \cdot 10^{17}$	$4.5 \cdot 10^{-4}$	$8.5 \cdot 10^{4}$	2.4
Our data	0.35μ	n	ΔN wi, si				7.4
Our data	0.35μ	p	ΔN wi, si				7.4

Table 4: Flicker noise experimental results summary.

Another example of a technological parameter influencing the noise is the gate material. It is shown in [1], [32] that a p-MOS with p^+ poly gate 'surface channel' is noisier than the n^+ or Al gate p-MOS. This is not a surprise since it has been intuitively known for long time that a p-MOS with a standard single n^+ polysilicon gate has lower noise than n-MOS because of its 'buried' channel or 'bulk' device behavior comparing to the n-MOS that is more a surface nature device.

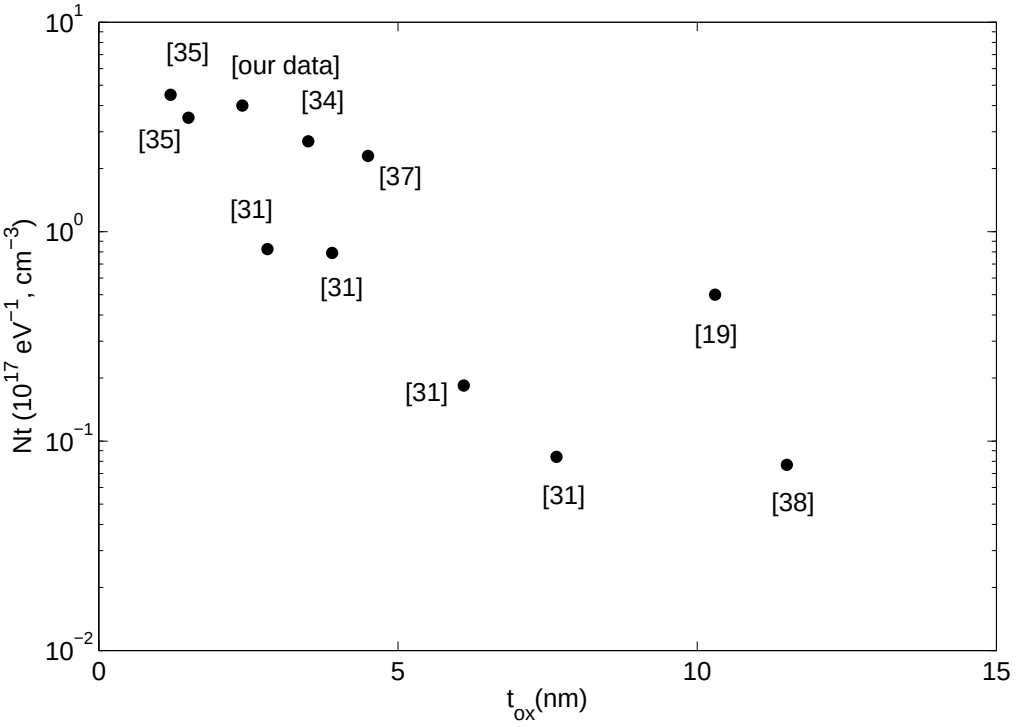

Figure 17: Technology scaling influence, N_t versus t_{ox} for n-MOS from literature.

It has also been shown by several authors (Vandamme, [11], [33]) that a series resistance of a LDD (lightly doped drain, used to reduce the maximum field near the drain) increases $1/f$ noise particularly for high biases. Lower noise is obtained by making the LDD shallow. The series resistance and the noise can on the other hand be reduced by silicidation. A method for extraction and calculation of the series resistance noise is explained for example in [33], [34]-[35]. Beside the series drain resistance causing the $1/f$ noise, in transistors with a small oxide thickness, a leakage gate current contributes significantly to $1/f$ noise.

In the early days of $1/f$ noise investigation, it was believed that α_H was a constant, nowadays it is accepted as a material parameter depending on the quality of a material. For high quality materials, i.e. high crystallinity, α_H has a low value. On the other hand, bad quality materials have a lot of defects what increases α_H and $1/f$ noise. The measured values for α_H of silicon span from $5 \cdot 10^{-6}$ to $2 \cdot 10^{-3}$ as known from the literature [32] and what can be confirmed by our experimental data summary in Table 4.

A large amount of experimental data can be found in literature, but often it is difficult to compare results. It is clear that it is difficult to compare different noise data due to different processing steps for different technologies, but it is also difficult because there are several different noise mechanisms and the model for each of them has restrictions concerning the biasing conditions and the device type. Further more, authors show different noise data S_{I_D}, S_{I_D}/I_D^2 or S_{V_g} as a function of drain current or gate voltage. In the ITRS roadmap [40], a figure of merit presented is input referred noise

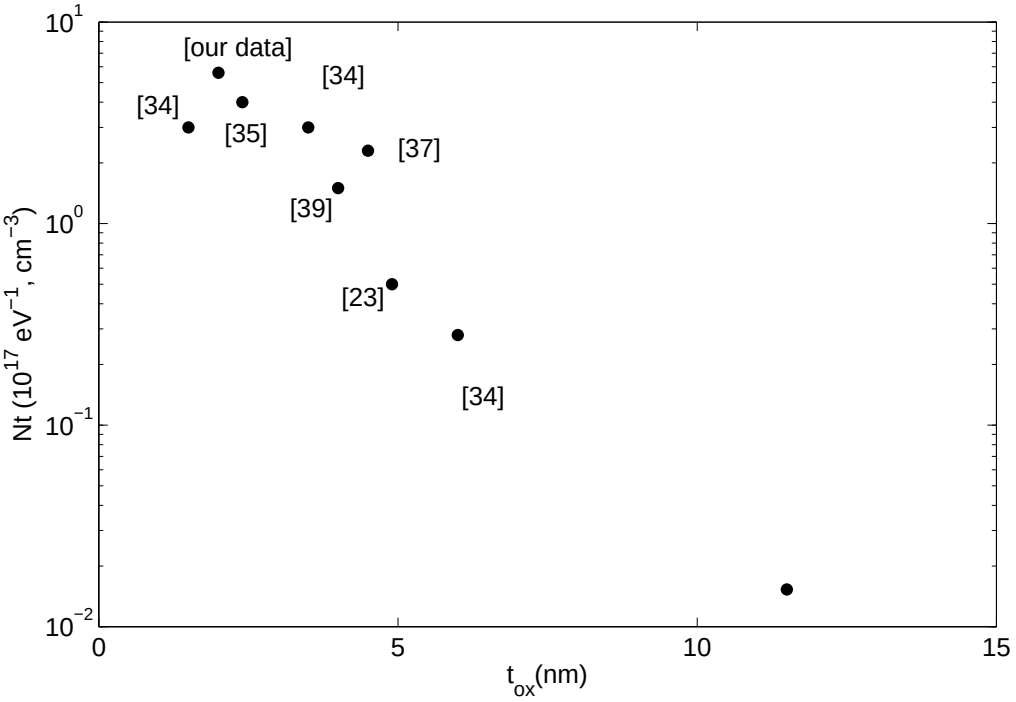

Figure 18: Technology scaling influence, N_t versus t_{ox} for p-MOS from literature.

spectral density at one Hertz times device area as a function of t_{ox} with the input noise calculated as $S_{V_g} = KF/(C_{ox}^2 WLf)$. However as it has been previously explained, this SPICE model used is oversimplified and is only valid for noise caused by the number fluctuations in ohmic region and can therefore not be used for other regions and for transistor with mobility fluctuations noise that is proportional to C_{ox}^{-1} and is gate bias dependent (see Table 3).

An obviously more appropriate figure of merit for comparison of noise of transistors from different technology nodes is a comparison of the oxide trap density N_t extracted from the weak inversion measurements. One of the arguments in favor of using this parameter is that most of the measurement data for weak inversion show consistent ΔN behavior and the other is that that is a parameter describing physical processes creating noise. Plots of N_t versus t_{ox} for n-MOS and p-MOS transistor generations from literature (Table 4) are shown in Fig. 17 and Fig. 18 respectively. Noise increase for reduced oxide thicknesses is obvious. Our data results are in line with the shown experimental data trend.

5.4 Noise Fluctuations

$1/f$ noise is a phenomenon showing large statistical variations, measurements show different results from devices on the same die, and even for the same device under different operation regions. For small devices, with visible Lorentzian spectra, the RTS noise of a small number of traps is a dominant noise mechanism. Due to this small number of traps, the measured statistical variations of noise can be even greater than an order of magnitude [22]. Manufacturing process variations of the conduction parameters (C_{ox}, V_T, W and L) show minor impact on the noise variation, while the dominating influence on the noise fluctuations is from the number of traps randomly distributed in the gate and

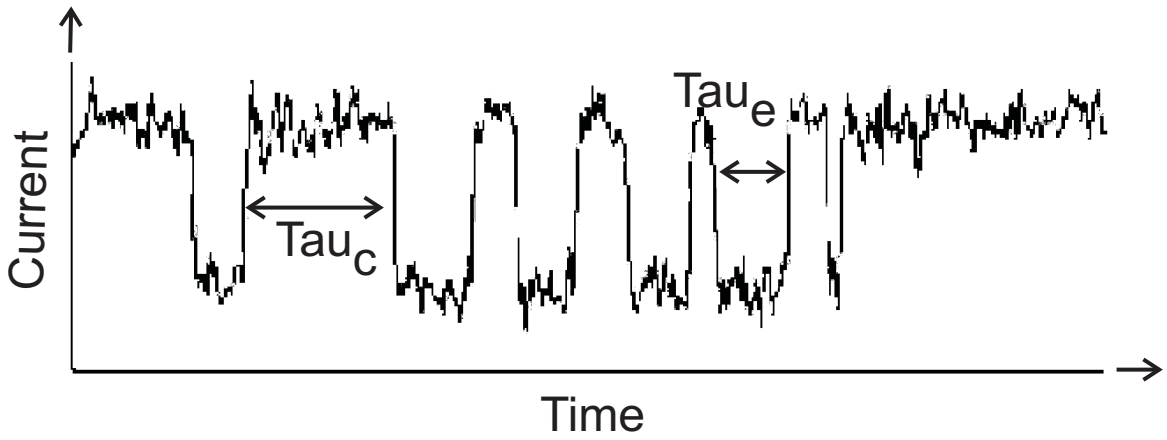

Figure 19: Drain current in the time domain with visible RTS.

at the S_i-SiO_2 interface, N_t.

Not much work has been devoted to the modeling of statistical effects of $1/f$ noise. Some statistical models are described in [41]-[42]. First time in [43] (2005) a statistical nature of $1/f$ noise has been implemented in a circuit simulator (BSIM) based on measurements from 200 devices from a $0.18\mu m$ technology. It has been shown that the smaller area devices have a larger spread and that the standard deviation of the number of traps has $1/\sqrt{WL}$ dependence which is in line with the conclusion from [42].

5.5 RTS and Switching Effects

In small area MOS transistors (typically with area less than $1\mu m^2$) it is possible to observe random telegraph signals RTS caused by a single carrier trapping-detrapping at the interface. A time domain plot of the RTS signal is shown in Fig. 19. Transition times from low to high level are random variables with Poisson distribution ($t_c \sim exp(-t/\tau_c)$ and $t_e \sim exp(-t/\tau_e)$) and time constants capture time τ_c and emission time τ_e represent average values of the high and low time constants respectively. Fluctuations of a singe trap cause the drain current spectral density with a Lorentzian spectra described by [22]

$$S_{I_D} = 4A\Delta I_D^2 \frac{\tau}{1+\omega^2\tau^2} \tag{126}$$

where $\tau = (1/\tau_c + 1/\tau_e)^{-1}$, $A = \tau/(\tau_c + \tau_e)$ and ω angular frequency $2\pi f$. An approximated formula for calculating the amplitude of the RTS drain current is given by

$$\frac{\Delta I_D}{I_D} = \frac{g_m}{I_D}\frac{q}{WLC_{ox}}\left(1 - \frac{d}{t_{ox}}\right) \tag{127}$$

with d being distance of the trap to the $Si - SiO_2$ interface. From this formula it can be seen that the RTS noise amplitude varies as g_m/I_D. RTS noise is in principle ΔN noise and this dependence is in line with the method for determining the origin of $1/f$ noise based on the observation of the drain current PSD as a function of the transconductance to I_D ratio.

As explained when dealing with the ΔN noise theory, summation of the RTS with the right distribution of time constants gives $1/f$ noise and it is strongly believed that the RTS noise is one

of the fundamental noise components. The observations of the individual traps for small devices and extraction of RTS noise parameters, have given a strong support to the ΔN model.

A study of the RTS noise under high periodic signal excitation has gained increased attention in the later years because of the observed phenomenon that $1/f$ noise reduces in a MOSFET when a periodic large signal is applied to its gate. This was observed for the first time in [44] and during the last seven years several authors have measured and analyzed this phenomenon. It can be calculated that the drain current PSD decreases 6dB when applying a periodic gate-source bias voltage with 50% duty cycle due to a transistor being active only half of the time. In their measurements, the authors observed an additional noise reduction at frequencies lower than the switching when cycling MOS from inversion to accumulation. In [45] extra 5-8dB is reported at 10Hz independent on the switching frequency. The reduction was shown to depend on the accumulation (off) voltage and it was noticed that the Lorentzian (RTS) spectra disappeared when switching. In [46] it was also shown that for small devices noise increases for some transistors and that the reduction is observed on average.

When a transistor is switched on and off with a period that is faster than the emission and the capture time constants of the traps τ_e and τ_c, the traps can not follow this fast oscillation and their occupancy or in other words their trapping and de-trapping activity changes comparing to the steady-state case occupancy. So the effective time constants of all RTS in the sample will change comparing to the steady-state and the on time constants will be $\tau_c \cdot m_c$ while the off time constant will be τ_e/m_e [47]. It is suggested that these time constants vary periodically and the switching noise is treated as cyclostationary RTS noise. To explain the observed noise reduction, authors explain that the distribution of τ of the traps is not uniform in $\log t$ [48]. They suggest that the trap density deeper in the bandgap is lower and that it is these traps that contribute to the noise when switching the transistor on and off giving reduced noise.

Modeling of the switched noise behavior is described in some newer works by authors from Infineon and Delft University [49], [50]. However no simulator implementation of the switched bias phenomenon exist.

Switched biasing is considered a method to decrease a circuit noise interfering with the physical properties of a device. Besides its use in low-frequency circuits, it is also beneficial for high-frequency circuits where $1/f$ noise is upconverted to higher frequencies. Some applications of this principle exist, for example an amplifier with reduced noise due to switching is shown in [51] and an oscillator in [52]. A very recent overview of the switching phenomenon is given in [48] with some circuit implementation examples.

Besides practical circuit applications, this phenomenon can also give new insights into the $1/f$ noise physics mechanism that has traditionally been studied only in a steady-state operation. In [53] comparison of the impact of hot-carrier degradation on noise for a steady-state and a periodic bias is given for n-MOS. Usual increase of N_t and thus $1/f$ noise due to hot-carrier stress is even more pronounced for switched bias than steady state bias, and the noise reduction due to switching diminishes. Other measurement data on p-MOS from [54] show that larger noise reduction can be achieved with devices having larger t_{ox}. Transistors from the same paper follow $\Delta\mu$ model in all regions, non-usual for a p-MOS.

In our measurements no reduction due to switching was observed for transistors from fab A at 10kHz.

Another method for reducing the $1/f$ noise based on the inherent transistor properties might be based on the work presented in [55]-[56] where it is shown that $1/f$ noise is decreased 50% if a body of a transistor working in weak inversion is forward biased. This observation opens a possibility to design an amplifier with reduced noise if forward body bias is applied to the input transistors working in weak inversion, which is risky for a product but might be done for research. The explanation for this phenomenon is found in the McWhorter theory and as this reduction principle relies on the fact that the noise in weak inversion is caused by the ΔN mechanism, it is first needed to confirm that the noise origin is ΔN in the technology used.

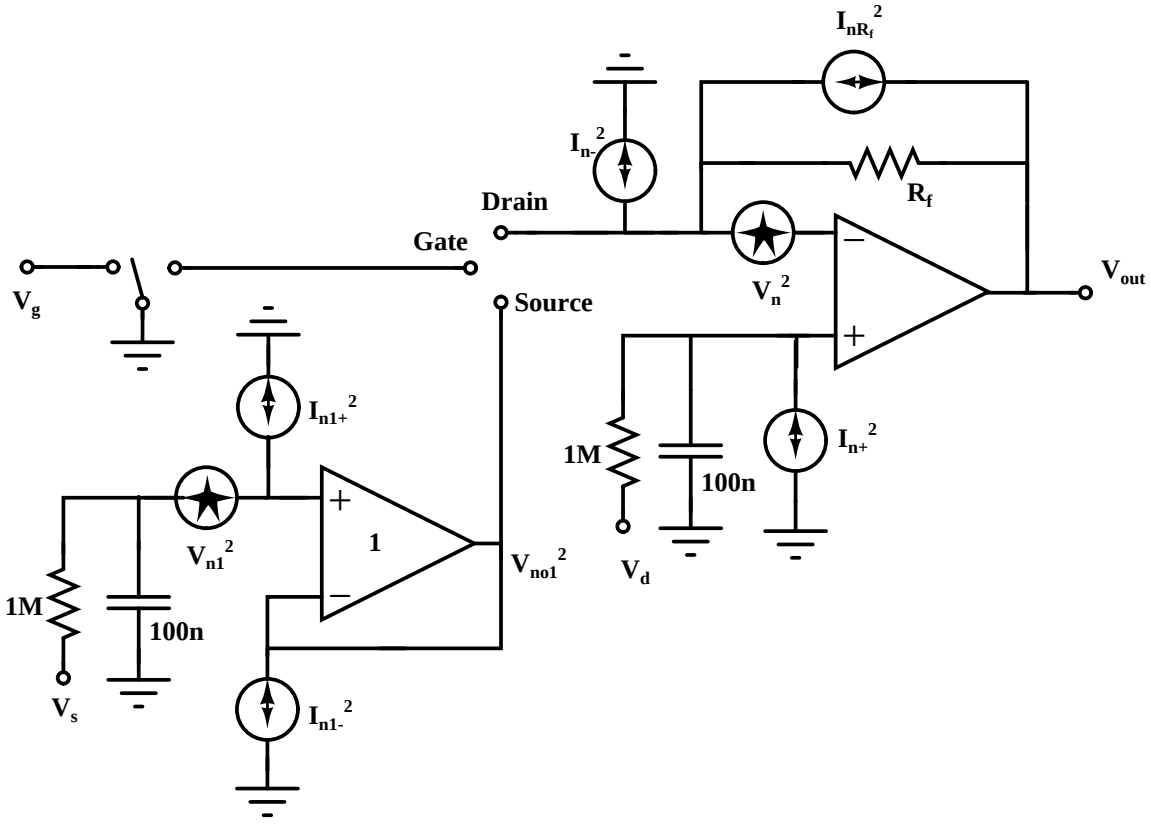

Figure 20: Noise measurement set-up.

5.6 Noise Measurement Results

Noise has been measured on transistors from two different technologies. Transistors from fabricator A have minimum size $0.13\mu m$ and transistors from fab B have minimum size $0.35\mu m$. The transistors have been tested in both weak and strong inversion and in both linear and saturation regions. From the measurement data noise origin has been determined for all the devices and the physical parameters have been extracted for the $0.13\mu m$ technology. Comparison with the simulations is also shown for both technologies. For simulations for the transistors from fab A, BSIM3v3 noise model was used, while for the transistors from fab B only SPICE model parameters were available.

5.6.1 Measurement Set-Up

Measurement set-up used is shown in Fig. 20. For amplifying the drain current noise of the tested devices a low-noise amplifier AD707JN connected in a transconductane configuration has been used. Measurements have been performed for different transistor bias voltages supplied from a PC. The amplifier has been biased using batteries. For providing the variable transistor bias voltage values and performing measurements, a NI6289 high-precision data acquisition card has been used. Noise spectra and communication with the card have been obtained with help of NI software. The measurement

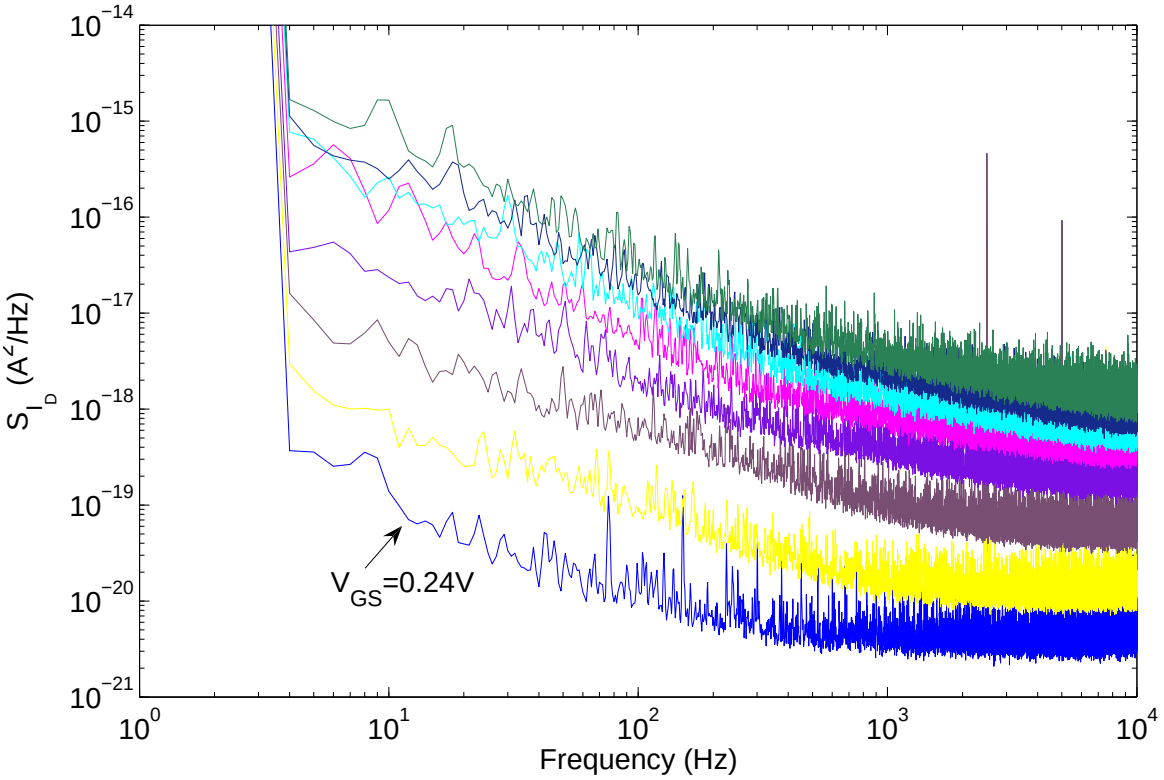

Figure 21: A typical noise spectrum for different bias voltages, V_{GS}=0.24V to V_{GS}=0.52V in 40mV step, for $10\mu m/0.5\mu m$ n-MOS transistor from $0.13\mu m$ technology, V_{DS}=0.45V.

system noise can be calculated from Fig. 20 as

$$V_{no}^2 = \frac{R_f^2}{r_{ds}^2} V_{no1}^2 + R_f^2 I_{DSn}^2 + R_f^2 I_{R_f}^2 + R_f^2 I_n^2 + R_f^2 V_n^2 \left(\frac{1}{R_f} + \frac{1}{r_{ds}} \right)^2 \tag{128}$$

with r_{ds} being transistor drain-source resistance, I_{DSn} transistor drain noise current, V_n and I_n amplifier noise voltage and current respectively. Calculated noise using (128) matches measurements with a resistor of known value used as a DUT.

The transistors tested from both technologies have width W=10μm and different lengths. Different size transistors have common gate, source and bulk connections and separate drain. Prior to noise measurements, DC characteristics $I_D(V_{GS})$ and $g_m(V_{GS})$ have been measured. As explained in [57], from the DC characteristics for V_{DS}=50mV using the function

$$\frac{I_D}{\sqrt{g_m}} = \left(\frac{W}{L} C_{ox} \mu_0 V_{DS} \right)^{\frac{1}{2}} (V_{GS} - V_{th}) \tag{129}$$

the conduction parameters μ_0, V_{th}, ΔL and S

$$S = (\frac{dlogI_D}{dV_{GS}})^{-1} = 2.3 \frac{kT\eta}{q} \tag{130}$$

can be extracted. The values of the conduction parameters extracted for 0.13μm p- and n-transistors are given in Table 5.

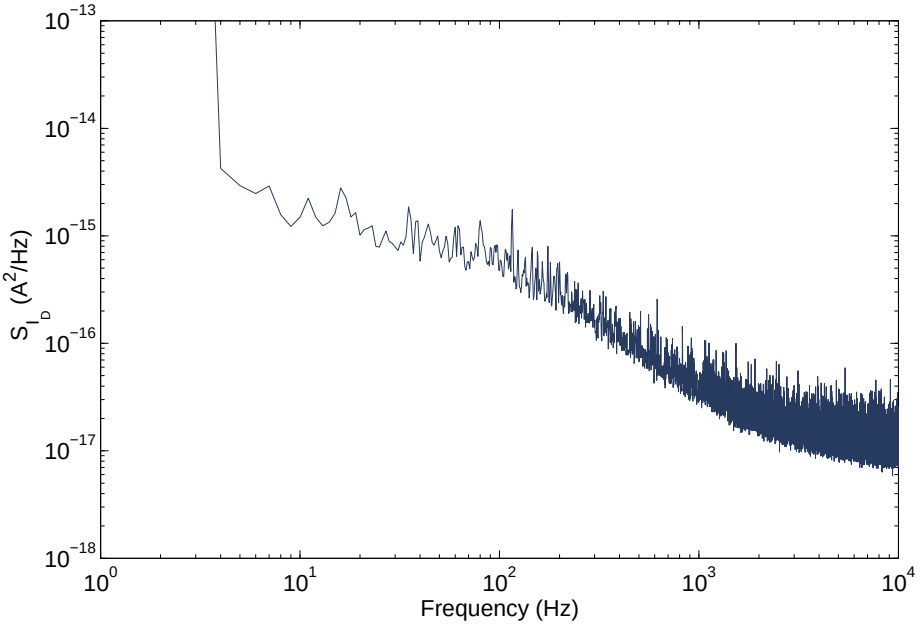

Figure 22: Lorentzian like spectrum of a small area $10\mu m/0.13\mu m$ n-MOS device.

L (μm)	0.13	0.26	0.5	1	2
$V_{thn}(V)$	0.41	0.395	0.372	0.360	0.336
$V_{thp}(V)$	0.365	0.364	0.353	0.349	
S_n (mV/dec)	86.23	84.97	84.19	95.7	97.05
S_p(mV/dec)	96.32	87.62	91.66	92.6	
ΔL_n (μm)			0.01		
ΔL_p (μm)			0.015		
μ_{0n} (cm^2/Vs)			221		
μ_{0p} (cm^2/Vs)			60		

Table 5: Extracted transistor conduction parameters (W=10μm) for n- and p-MOS from 0.13μm process

5.6.2 Results Discussion

Firstly, the noise data for the 0.13μm technology will be analyzed, afterwards they will be compared to the measurements from fab B in 0.35μm technology. A typical noise spectrum for different bias voltages for $10\mu m/0.5\mu m$ n-MOS transistor from the $0.13\mu m$ technology is shown in Fig. 21. A spectrum of a small area $10\mu m/0.13\mu m$ n-MOS device with a Lorentzian shape is shown in Fig. 22. In all the data presented, this type of spectra usually observed on the top of $1/f$ noise for small area devices have not been taken into account. The results presented in the further text, show PSD measured at 1Hz. For 0.13μm the same noise behavior has been observed on three measured samples and the results from only one of them will be presented. 0.13μm technology devices have oxide thickness 2.4nm, n+/p+

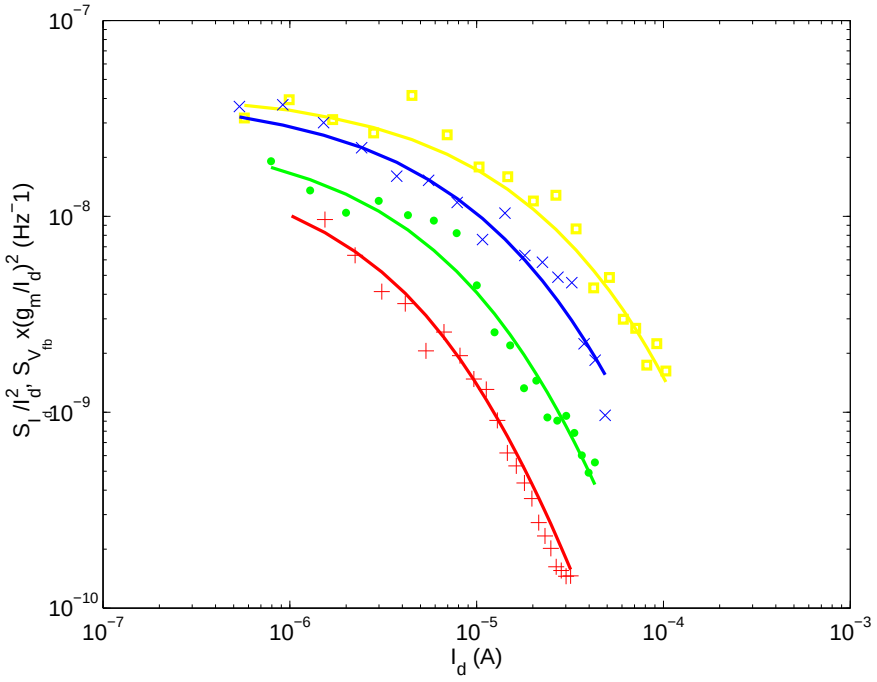

Figure 23: Normalized drain current noise S_{I_D}/I_D^2 and $(g_m/I_D)^2$ ratio (-) versus drain current for V_{DS}=50mV for n-MOS with various transistor lengths. L=0.13 ($\circ$), 0.26 ($\square$), 0.5 ($\times$), 1 ($\bullet$) and 2 (+) μm.

poly gate, shallow trench isolation and Co-silicided drain, source and gate.

To determine between the noise mechanisms involved in generating device noise, a plot showing the normalized drain current power spectral density S_{I_D}/I_D^2 in ohmic region and the corresponding $(g_m/I_D)^2$ ratio versus transistor drain current is usually used [22]. This plot is shown in Fig. 23 for n-transistors for several dimensions and in Fig. 24 for p-transistors for several dimensions. As it was shown by (98), if there is a good correlation of the drain current noise with the corresponding transconductance to drain current ratio squared, the number fluctuation model dominates. On the other hand, if this two curves are uncorrelated, an additional noise mechanisms exist. In our measurements, a good correlation is observed for n-transistors, while for p-transistors a departure from the $(g_m/I_D)^2$ characteristics in strong inversion can be explained by the influence of the additional correlated mobility fluctuation. In weak inversion, a plateau is observed for both types of devices showing that the drain current PSD has a quadratic dependence of drain current as it is predicted by the number fluctuations model. Based on this a formula

$$S_{I_D} = \frac{q^4 N_t}{kTWL\gamma C_{ox}^2 \eta^2} \frac{I_D^2}{f} \tag{131}$$

can be used for extracting the oxide trap density N_t. A value of the weak inversion slope factor η obtained from the DC measurements and shown in Table 5 is used in the formula. For both types of devices, the value of N_t is about $3 \cdot 10^{17} - 4 \cdot 10^{17} (eV^{-1} cm^{-3})$. N_t extracted from the measurements in strong inversion for n-transistors using the strong inversion noise formula matches the value for weak inversion.

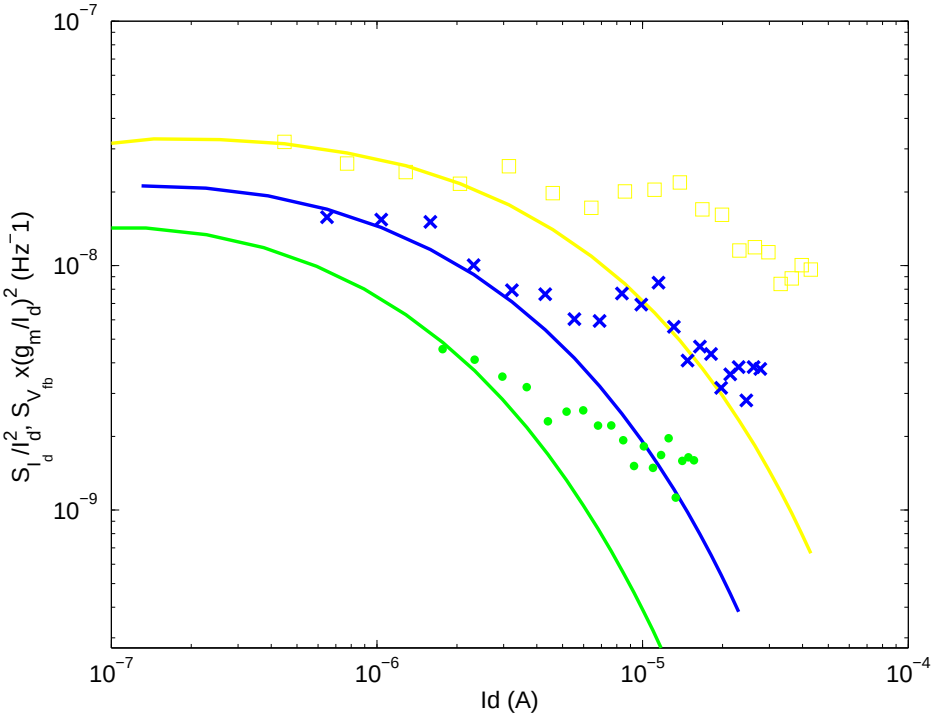

Figure 24: Normalized drain current S_{I_D}/I_D^2 noise and $(g_m/I_D)^2$ ratio (-) versus drain current for V_{DS}=50mV for various p-MOS transistor lengths. L=0.13 (○), 0.26(□), 0.5 (×) and 1 (•) μm.

Another method for determining the noise origin is plotting the input referred noise power spectral density as a function of the gate source voltage. In Fig. 25 the input noise is plotted as a function of the effective gate-source voltage for n-transistors and in Fig. 26 for p-transistors for V_{DS}=50mV. From these figures, the noise origin observed in Fig. 23 and 24 can be confirmed by the fact that the input noise does not depend on V_{GS} for n- transistors while it is proportional to V_{GS}-V_{th} for p-channel transistors. This is as predicted by the formulas (92) and (55) respectively. Sometimes observed S_{I_D} dependence on V_{GS} for high overdrive voltages due to the series resistance can not be observed for relatively low bias voltages in Fig. 25. The solid lines in Fig. 25 and 26 are results obtained by simulations. It can be seen that the simulator model predicts very well the noise of p-transistors, while discrepancies exist for the n-channel in linear region. The model predicts a dependance on the gate bias similar to a p-channel bias dependance. This might be due to the fact that for a correct modeling when the ΔN model dominates, similarly to α_H, the NOIB model should be proportional to $(V_{GS} - V_{th})^{-1}$ as explained in the subsection on BSIM model. Besides that, it can be seen in Fig. 25 that the model provides different value of the flatband voltage comparing to the measured.

The mean value of α_H for p-transistors with different dimensions is about $4 \cdot 10^{-4}$. This value is obtained from the measurement data by using a formula with S_{I_D} expressed as a function of I_D, V_{GS} that does not require the measurement of the mobility attenuation factor θ (3). The values of α_s for p-channel transistors, extracted using the equation (105) have the values $3 \cdot 10^5 - 9 \cdot 10^5$. The values

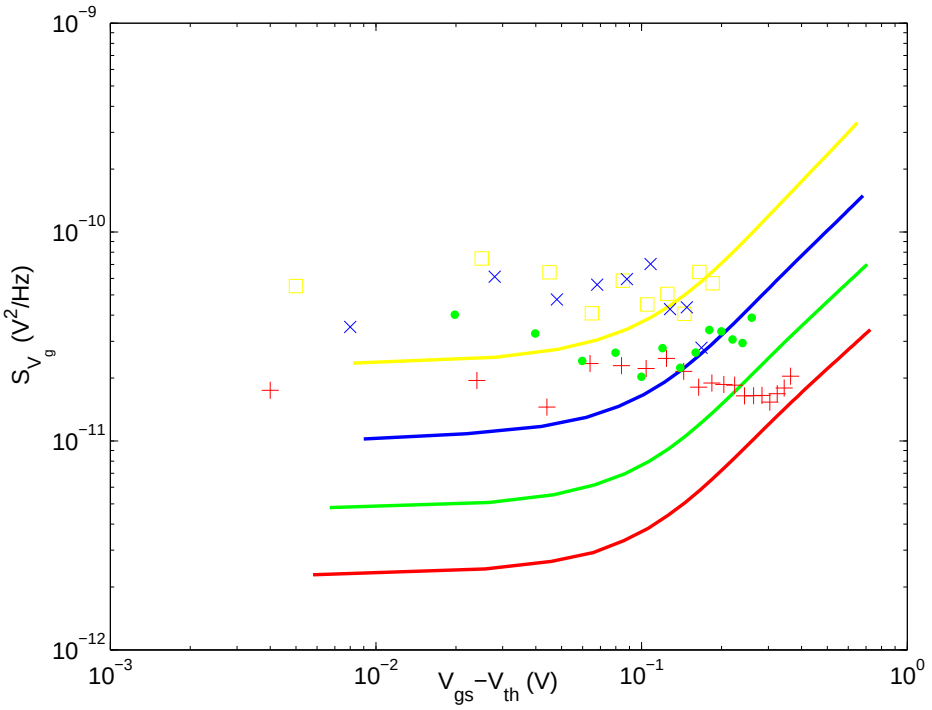

Figure 25: Input referred noise S_{V_g} versus gate overdrive voltage for V_{DS}=50mV for various n-MOS transistor lengths. Simulation (-), L=0.13 (∘), 0.26(□), 0.5 (×), 1 (•) and 2 (+) μm.

extracted are similar to the the values reported for the same technology node [34].

S_{I_D} versus drain current for V_{DS}=0.45V for various dimensions of p- and n-transistors is shown in Fig. 27 and 28 along with the simulated data. As expected, the drain current spectral density shows a quadratic dependence on the drain current in weak inversion for V_{DS}=450mV as for 50mV. Similarly to the data for transistors working in linear region, measurements for p-channel transistors match very well simulations while for n-transistors discrepancies are observed. The simulated results from Fig. 27 predict the same dependance on drain current as measured and the difference observed might be due to a batch to batch parameter variation.

After analyzing the first technology data A, we proceed with the data analysis of the 0.35μm technology B. Measured transistor dimensions are the same as for fab A and the same measurement setup has been used for both technologies.

In Fig. 29 the drain current PSD is plotted as a function of drain current for a 10μm/0.5μm transistor for V_{DS}=50mV and for V_{DS}=0.45V for n-transistors (upper two curves) and for p-transistors (lower two curves). As expected p-transistors have about one decade lower noise. It can be noticed that for both types of devices for lower drain currents (weak inversion), noise spectral density has quadratic dependance on the drain current for any value of the drain-source voltage. Going out of the subthreshold operation region, the curve for low V_{DS} departs from the one for saturation region for both n- and p-devices. This behavior in weak inversion confirms the results for the technology A and the majority of experimental data that the noise in weak inversion is due to ΔN model for both

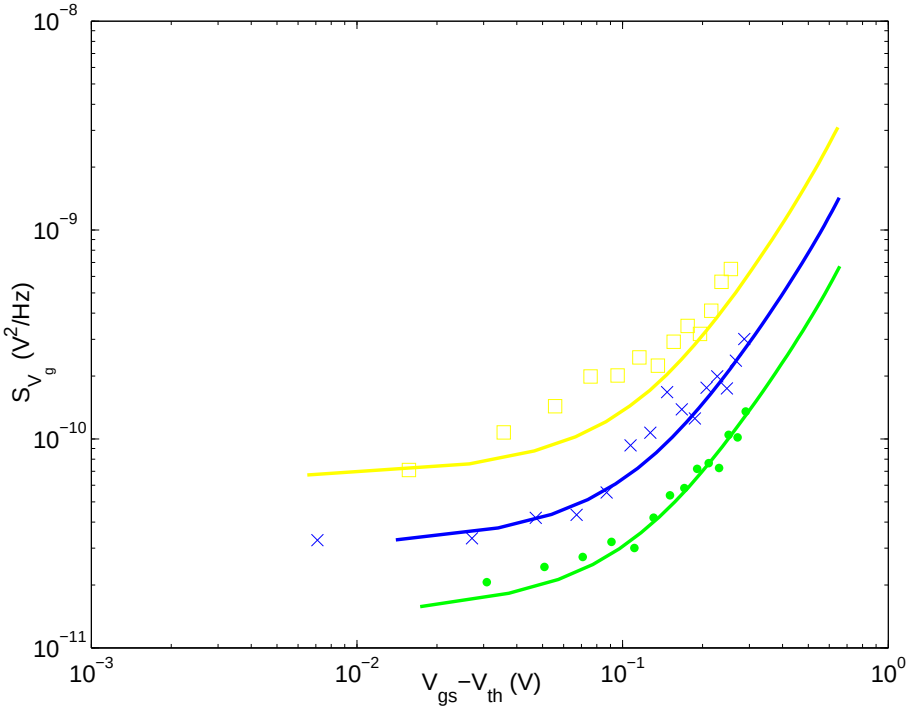

Figure 26: Input referred noise S_{V_g} versus gate overdrive voltage for V_{DS}=50mV for various p-MOS transistor lengths. Simulation (-), L=0.13 (∘), 0.26(□), 0.5 (×) and 1 (•) (+) μm.

types of devices. From the curves in strong inversion in linear region it can be seen that the noise PSD becomes constant for increased current. As explained before, this reveals that in this technology noise in both p- and n-transistors originates from the number fluctuation theory. This has been observed before, for example in [17], but is not the most common case. The most common case is that the noise of the p-channel transistors shows dependence on the gate bias according to the $\Delta\mu$ theory. That that is not the case here can be verified by plotting the input referred noise PSD as a function of the gate bias voltage (Fig. 30, input referred noise for 10μm/0.5μm n- and p-MOS, $V_{DS} = 0.45V$). It can be seen in the latter figure that both n- and p-MOS show similar dependance on the input voltage and no clear increase for p-transistors can be noticed contrary to what was observed for p-MOS from technology A. Even though technology A has smaller minimum device length expecting to give larger noise fluctuations among samples, different samples showed the same behavior, while the data from fab B show greater spread and therefore several samples' data are shown in Fig. 30. In the same figure, noise predicted by simulations is shown by full lines. It can be noticed that besides the fact that the simulated noise is greater than measured for the devices in strong inversion, the simulator can not predict a proper bias dependence for transistors in weak inversion. This is not surprising as the noise model used is a simple SPICE model (106), which as already explained can predict only ΔN noise in strong inversion. Unfortunately that was the only model provided by the foundry.

To compare further more the noise data from the two foundries, in Fig. 31, the drain current PSD as a function of I_D for n-transistor $10\mu m/0.5\mu m$ is shown for V_{DS}=50mV and for V_{DS}=450mV for fab

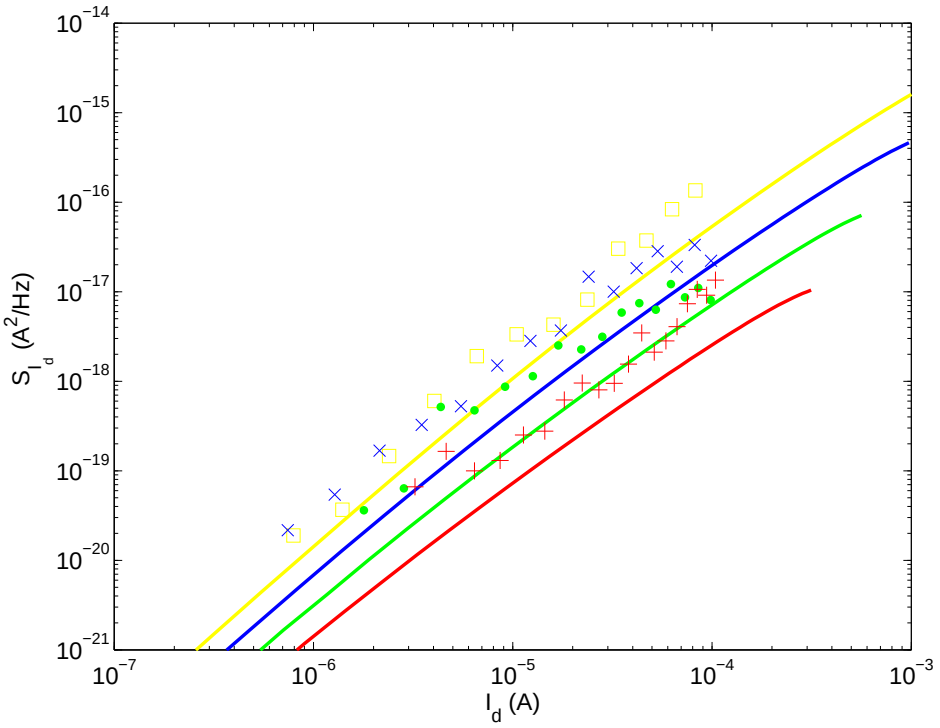

Figure 27: Drain noise spectral density S_{I_D} versus drain current for V_{DS}=450mV for various n-MOS transistor lengths. Simulation (-), L=0.13 (∘), 0.26(□), 0.5 (×), 1 (•) and 2 (+) μm.

A (light) and for fab B (dark). Full lines are simulated results. It can be noticed that the transistor technology with greater minimum size device has less noise in strong inversion, and more noise in weak inversion for the same current through the devices comparing to the fab with minimum size device $0.13\mu m$. In the ohmic region the noise current is constant for greater bias in both cases, i.e. ΔN model dominates for n-MOS for both technologies.

The plot corresponding to Fig. 31 for p-transistors is shown in Fig. 32. Again the dark curve is the noise of a device B with dimensions 10μm/0.5μm in linear (V_{DS}=50mV) and saturation region (V_{DS}=450mV) and the light curve is the noise of a 10μm/0.5μm device from fab A in linear and saturation region. Comparing the two technologies, it can be noticed that the noise of the p-MOS of fab A increases with increased bias current in both regions, while it saturates in the linear region for fab B. As explained previously, this is because the noise of p-transistors of these two technologies has a different origin. While the noise of the transistors of fab B is due to number fluctuation model, the transistors A show noise due to mobility fluctuations in strong inversion. In weak inversion, noise is ΔN in both cases. It can be also noticed, that the noise of the p-device in 0.35μm technology is much less than the noise of the p-device in 0.13μm technology or comparing with Fig. 31 that a p-MOS from fab A is almost as noisy as the n-MOS from the same technology. Traditionally p-MOS has been known for its low-noise because of its buried channel behavior. However in newer technologies, similar to the one used here, it has been shown that a p-MOS with p^+ poly gate 'surface channel' is noisier than a traditional n^+ or Al gate p-MOS [1].

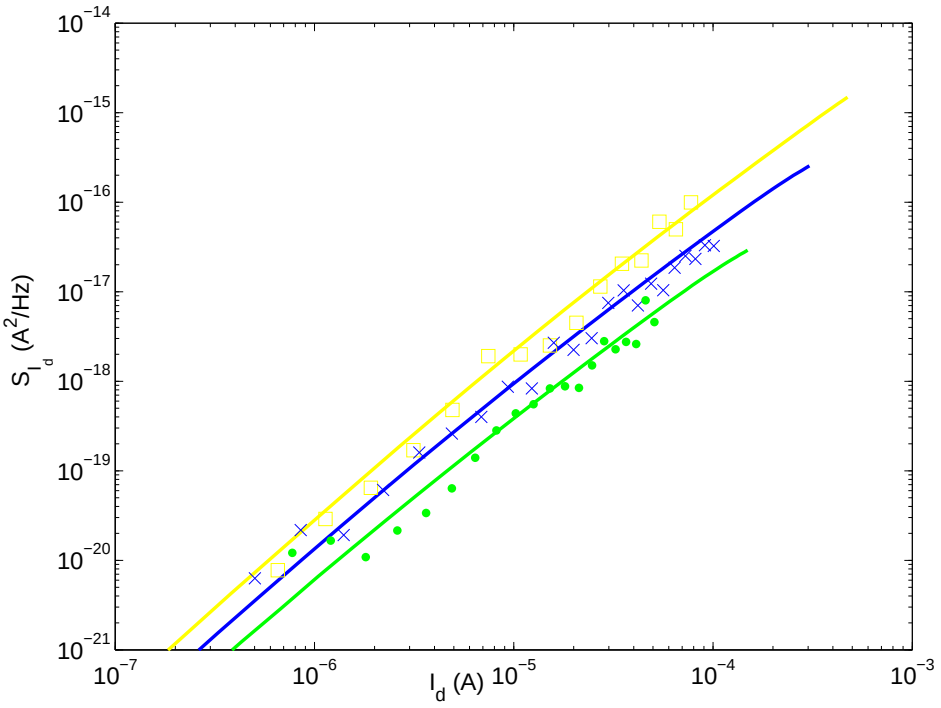

Figure 28: Drain noise spectral density S_{I_D} versus drain current for V_{DS}=450mV for various p-MOS transistor lengths. Simulation (-), L=0.13 (○), 0.26(□), 0.5 (×) and 1 (•) μm.

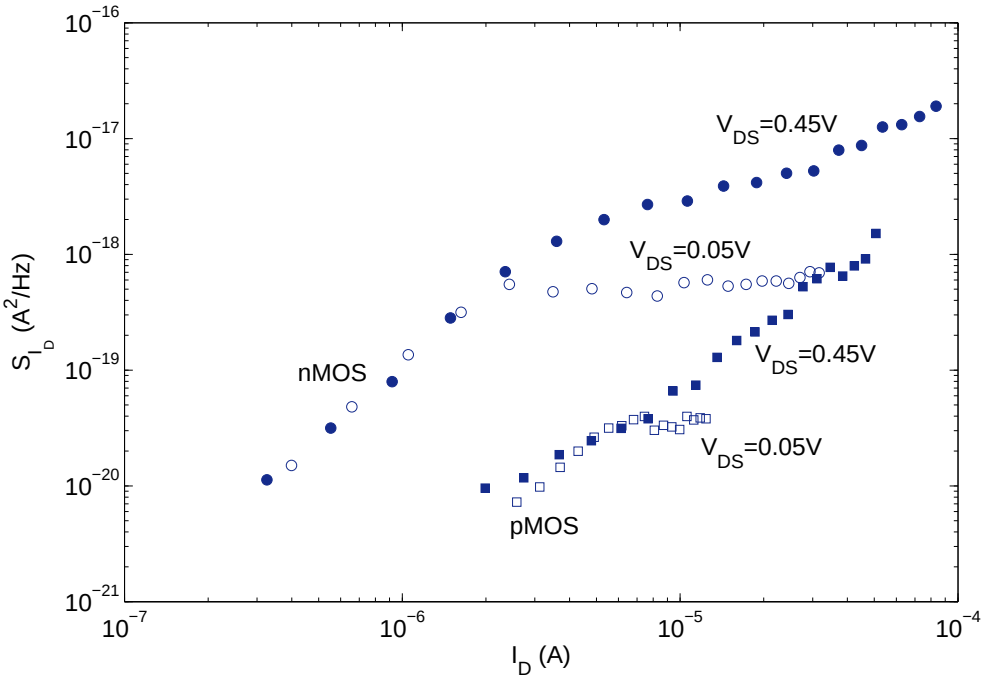

Figure 29: Drain noise spectral density S_{I_D} versus drain current for V_{DS}=450mV and for V_{DS}=50mV for 10μm/0.5μm n-MOS (upper two curves) and p-MOS (lower two curves) from fab B.

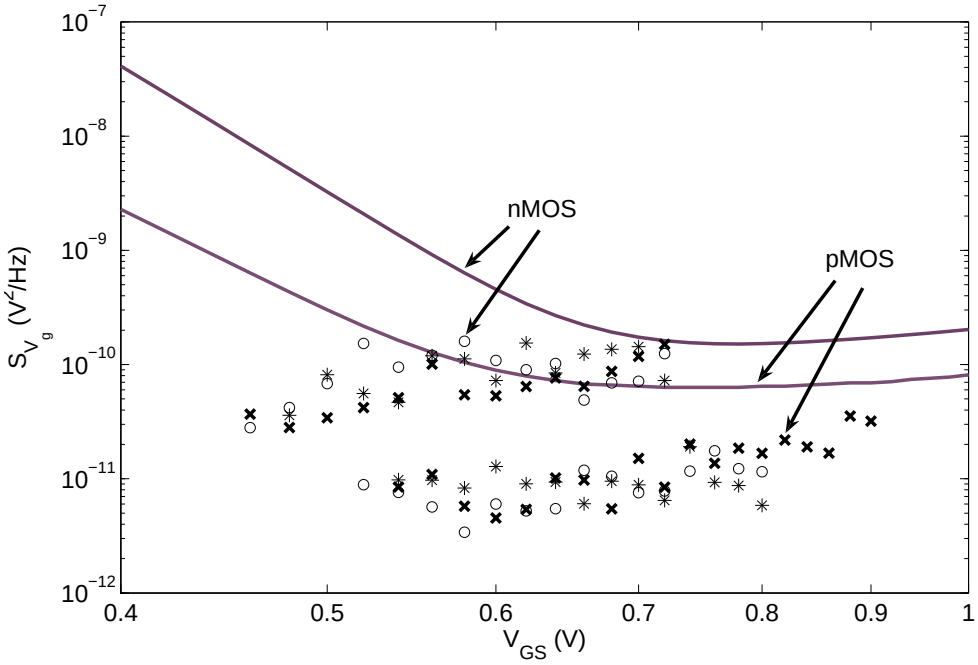

Figure 30: Input referred noise S_{V_g} versus V_{GS} for V_{DS}=450mV for $10\mu m/0.5\mu m$ n-MOS and p-MOS transistors from fab B. Full lines are simulation results (SPICE).

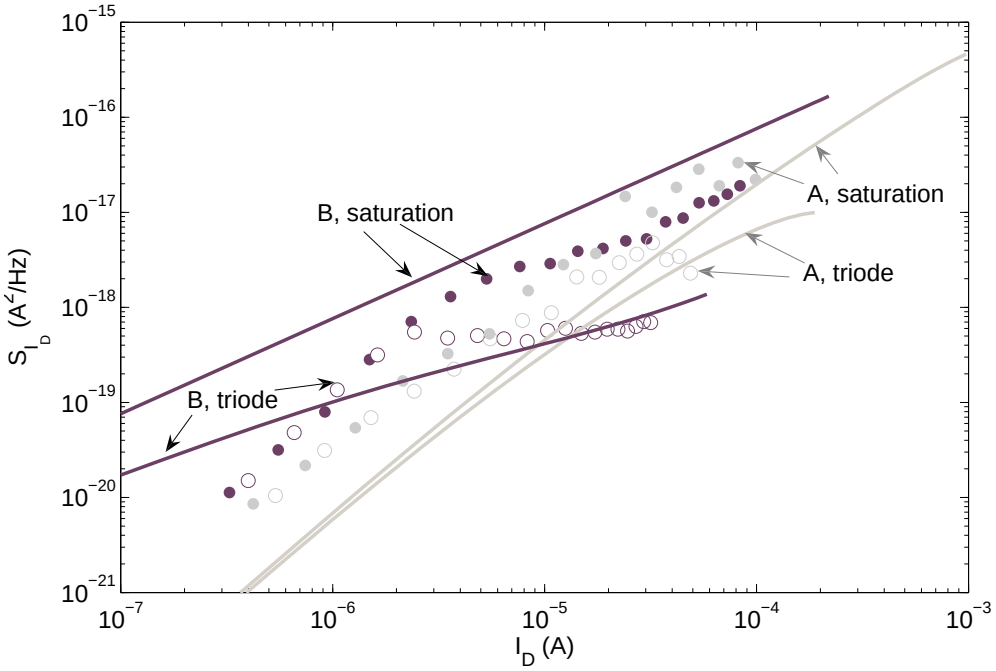

Figure 31: Drain noise spectral density S_{I_D} versus drain current for V_{DS}=450mV and for V_{DS}=50mV for $10\mu m/0.5\mu m$ n-MOS transistors from fab A (light) and fab B (dark). Full lines are simulation results (fab A BSIM, fab B SPICE).

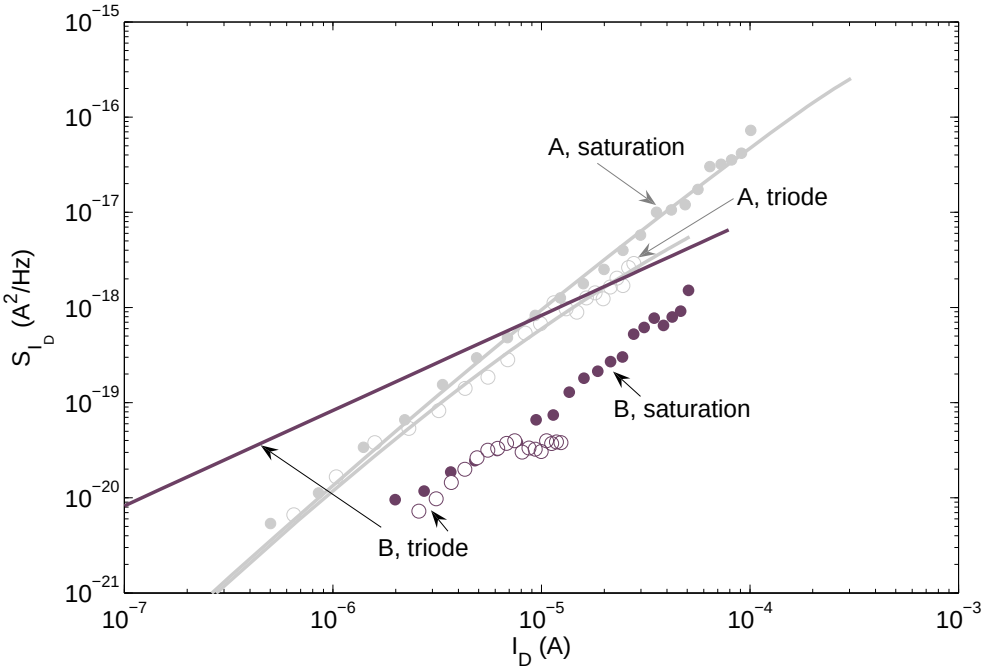

Figure 32: Drain noise spectral density S_{I_D} versus drain current for V_{DS}=450mV and for V_{DS}=50mV for $10\mu m/0.5\mu m$ p-MOS transistors from fab A (light) and fab B (dark). Full lines are simulation results (fab A BSIM, fab B SPICE).

5.6.3 Gate-leakage and Drain Resistance Current Noise

In new technologies with downscaling, gate-leakage current and drain resistance noise influence become significant. To demonstrate this effect Fig. 33 is borrowed from [35]. In that figure S_{I_D} and S_{I_D}/I_D^2 versus I_D are shown for n-MOS transistors from ST Microelectronics fabricated in 45nm and 30nm technology. Apparently the gate noise has very pronounced influence.

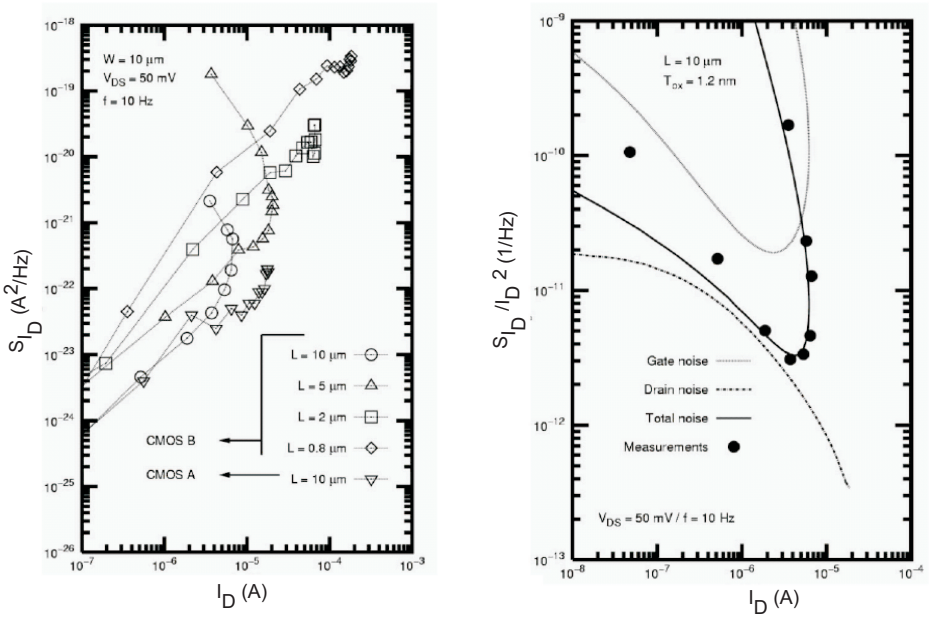

Figure 33: S_{I_D} and S_{I_D}/I_D^2 in the ohmic region versus drain current for 0.45nm, t_{ox}=1.5nm (A) and 0.35nm, t_{ox}=1.2nm (B) n-MOS. The figure is taken from [35].

6 Conclusion II

In this chapter, an overview of the existing theories explaining transistor $1/f$ noise origin has been presented. Derivation of the formulas showing physical noise parameters and transistor parameters dependance has been summarized. Some improvements proposed in the literature of the usually used noise formulas have been mentioned while investigating weaknesses and incompleteness of the existing models. An overview of the simulator models has been given as well. Experimental data from the literature have been collected, summarized and some conclusions drawn. Finally our experimental results for two technologies have been described and compared with simulations. The experimental part of this work demonstrates how noise can be measured and analyzed and how the noise parameters can be extracted from the noise data. It reveals that a priori noise origin is difficult to know which is what complicates the noise modeling. It also shows that it is difficult to compare noise from different technologies and that a lot of measurements is necessary for a proper noise model. The statistical nature of noise makes modeling even more difficult, what has also been demonstrated. Some general observations of the influence of technology scaling on noise have been presented and experimentally verified and some new research areas and phenomena such as switched transistor noise have been mentioned. Lastly, since the noise model is usually provided to a designer by a foundry, this experimental work reveals relevant information to a designer about how characterization and modeling should be done and what level of confidence in the model provided one can have. However, this overview clearly

shows that despite its long research tradition, with constant process changes and scaling $1/f$ noise will still remain a task to explore. In the next part of this thesis we will apply the knowledge on noise gained by now and physical noise parameters obtained by the extraction methods described here to optimize a preamplifier for a capacitive source (i.e. condenser microphone).

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7 Noise Optimization of Preamplifiers for Capacitive Microphones in CMOS

In this chapter of the thesis we apply previously described transistor noise analysis to a problem of noise optimization of a preamplifier for a capacitive microphone.

CMOS circuitry is easily integrated with increasingly popular capacitive MEMS microphones. In addition to sensing the microphone signal, CMOS electronics provides microphones with new functionalities such as a digital output. Evolution of CMOS technology with transistor size scaling allows increased functionality in a small silicon area. If the microphone has negligible intrinsic noise, in a properly designed front-end, a signal-to-noise ratio (SNR) is limited by the input transistor noise. Optimization of a microphone preamplifier input transistor, done with respect to sensor, is an important design task that includes choices of an optimal transistor type (p- or n-), choices of an optimal length L and width W as well as a choice of transistor operating point. Optimization is strongly dependant on transistor model parameters and can become a challenging task as submicron technologies are often developed and characterized for digital design.

A general noise optimization methodology for amplifiers with a capacitive source can be applied to a microphone preamplifier. An electret microphone preamplifier basic noise considerations for a traditionally used JFET are compared with MOSFET in [1]. Noise optimization procedure of amplifiers with capacitive sources is a well-known procedure, described in [2], where thermal noise and flicker noise described by a simple empirical formula have been optimized for an input transistor working in strong inversion in saturation. Noise optimization for charge amplifiers, which are also amplifiers with a capacitive source, with enhancements for thermal noise in moderate inversion region has recently been discussed in [3]-[4] using the EKV MOS model formulas. Enhancement for flicker noise taking into account its dependence on the pMOS overdrive voltage have been considered in noise optimization of charge amplifiers in [5]. Analog designers prefer empirical formulas for flicker noise optimization as the physics based $1/f$ noise models were complicated or not general enough [6]. Recently, in [6]-[7] relatively simple physics based flicker noise model formulas have been presented that are valid for any region (EKV model) of operation and describe the two existing flicker noise mechanisms.

In this work, we use the described EKV model formulas for noise optimization of a preamplifier for a MEMS microphone with a p-type input transistor. Thermal noise optimization has been revisited and flicker noise optimization has been done if a mobility fluctuation ($\Delta\mu$) model has been used as well as if a number fluctuation (ΔN) flicker noise model has been used. Flicker noise parameters oxide trap density N_t and Hooge parameter α_H extracted from measurement data as explained in the chapter on flicker noise have been used. Microphone total noise optimization with an A-weighting filter [8] has been analyzed for two technologies and an optimal transistor dimensions choice discussed. Calculations are done for a microphone with capacitance 5.6pF which is the value of the microphone used in this thesis.

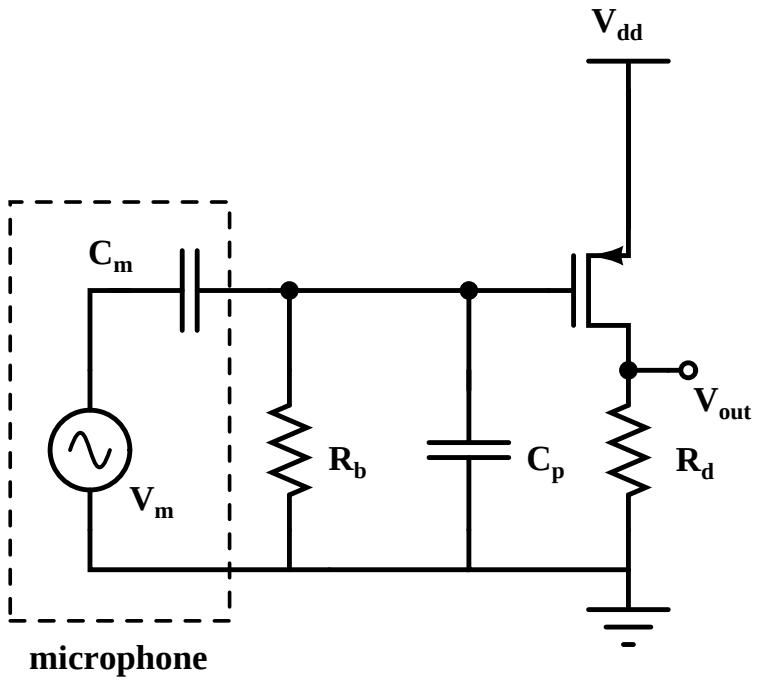


Figure 34: A simplified schematic of a microphone preamplifier.

7.1 Microphone Preamplifier Noise

A simplified schematics of a preamplifier with a microphone is shown in Fig. 34. Input referred noise, V_{ni}^2, referred to the intrinsic transducer source V_m, of a microphone and a preamplifier can be calculated as

$$V_{ni}^2(f) = V_{nm}^2 + \frac{I_{Dn}^2}{g_m^2}\left(\frac{C_m + C_p + C_g}{C_m}\right)^2 + \frac{4kT}{R_b\omega^2 C_m^2} + \frac{4kT}{R_{out}\cdot g_m^2}\left(\frac{C_m + C_p + C_g}{C_m}\right)^2 \qquad (132)$$

where V_{nm} is the microphone intrinsic noise, I_{Dn} is the transistor drain current power spectral density, g_m is the transistor transconductance, C_p is a parasitic capacitance seen between the transistor gate and ground and C_g is the gate capacitance of the input transistor. $4kT$ and ω have their usual meaning, R_b is a bias resistance from the transistor gate to ground and R_{out} is the amplifier output resistance $R_d \parallel r_{ds}$ where r_{ds} is the amplifier output resistance.

For achieving a maximum SNR (equal $20 \cdot log\frac{V_m}{V_{ni,rms}}$), the preamplifier input referred noise needs to be minimized. Neglecting the microphone noise, and disregarding the noise contribution of R_{out} and R_b which are minimal in a proper design, the SNR of the system is typically limited by the strongly technology dependant transistor noise.

MEMS microphone capacitance is typically several pico Farad; all the calculations here are for a microphone with capacitance C_m=5.6pF and with parasitic capacitance due to microphone preamplifier interconnection C_p=0.5pF.

7.1.1 Microphone Preamplifier Noise Optimization Basics

For a transistor working in strong inversion, transistor gate capacitance C_g can be calculated as

$$C_g = \frac{2}{3} C_{ox} W L + 2 C_{OV} W \tag{133}$$

where C_{OV} is a gate-source and gate-drain overlap gate-diffusion capacitance per channel width. Transistor transconductance in strong inversion in saturation is

$$g_m = \sqrt{2 \mu C_{ox} \frac{W}{L} I_D} \tag{134}$$

μ is the channel mobility, C_{ox} is the gate oxide capacitance per unit area, W channel width, L channel length and I_D transistor drain current.

Transistor gate-referred noise ($V_{ng}^2 = \frac{I_{Dn}^2}{g_m^2}$) equal to the sum of thermal and flicker noise is

$$V_{ng}^2 = \frac{4kT\gamma}{g_m} + V_{ngf}^2 \tag{135}$$

where 4kT have their usual meaning and γ is close to $\frac{2}{3}$ for long-channel devices in strong inversion.

If the transistor flicker noise follows the number fluctuation (ΔN) theory, the input-referred flicker noise PSD in strong inversion in saturation V_{ngf} is [9]-[10]

$$V_{ngf\Delta N}^2 = \frac{K_{\Delta N}}{W L C_{ox}^2 f} \tag{136}$$

On the other hand, if the flicker noise is due to mobility fluctuation, the input-referred flicker noise PSD is bias dependant and can be expressed in strong inversion in saturation by

$$V_{ngf\Delta\mu}^2 = \frac{K_{\Delta\mu}}{W L C_{ox} f} (V_{GS} - V_T) \tag{137}$$

V_{GS} is a gate-source voltage, V_T threshold voltage, f frequency and $K_{\Delta N}$ and $K_{\Delta\mu}$ are technology dependant parameters.

In weak inversion, g_m is proportional to drain current, γ is close to $\frac{1}{2}$ and $C_g = \frac{\eta - 1}{\eta} C_{ox} W L + 2 C_{ov} W$ (η is a weak inversion slope factor). Flicker noise in weak inversion can be expressed by using equations from [9].

By differentiating the transistor noise with a microphone in (132) with respect to W and equating the derivative to zero simple formulas can be obtained for a transistor working in strong inversion in saturation [2]. Thermal noise for a transistor with a capacitive source working in strong inversion in saturation is minimal if

$$C_g = \frac{C_m + C_p}{3} \tag{138}$$

and ΔN flicker noise in strong inversion in saturation is minimized if

$$C_g = C_m + C_p \tag{139}$$

Noise minimum will then be

$$V_{ngf\Delta N,min}^2 = \frac{8}{3} \frac{K_{\Delta N}}{C_{ox} f} \frac{C_m + C_p}{C_m^2} \tag{140}$$

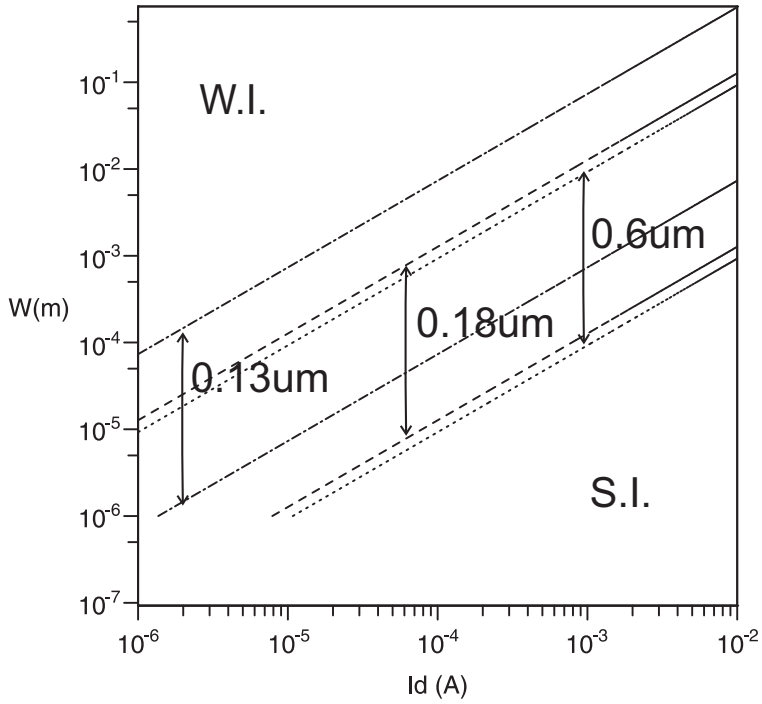


Figure 35: Moderate inversion limits for pMOS from technologies shown in Table 6 for a minumal transistor length.

7.2 Noise Optimization Enhancements Using EKV Model

Circuit designers widely use simple formulas for strong inversion presented so far. Moderate inversion region spans through two decades of transistor currents and is very important for applications where current consumption is limited; often, the input transistor of a front-end operate in moderate to weak inversion.

Moderate inversion region can be described by EKV model [7] which is based on relatively simple analytical expressions valid in all regions of operation. Additionally, the EKV model uses physical noise parameters for flicker noise modeling, while a commonly used BSIM3v3 MOS transistor noise model relies on non-physical fitting parameters non-convenient for hand calculation.

Transitions between the regions using EKV model (weak, moderate and strong inversion) are described by the inversion coefficient which is in saturation equal to

$$ifor = \frac{I_D L}{2\eta U_T^2 \mu C_{ox} W} \tag{141}$$

U_T is the thermal voltage. For $ifor < 0.1$ a transistor is in weak inversion, while for $ifor > 10$ it is in strong inversion; moderate inversion takes place for $0.1 \leqslant ifor \leqslant 10$. In Fig. 35 moderate inversion limits are shown for a minimum length transistor for pMOS technologies from Table 6 ($0.13\mu m$ CMOS, $0.18\mu m$ CMOS and $0.6\mu m$ thick oxide CMOS from a $0.18\mu m$ process). In calculations the slope factor η is assumed to be 1.3.

MOS	$L_{min}(\mu\text{m})$	t_{ox}(nm)	$\mu_0^*(\text{cm}^2/\text{Vs})$	$N_t(eV^{-1}cm^{-3})$	α_H	$C^*_{gso,gdo}(\frac{F}{m})$
n	0.13	2.4	280	$4 \cdot 10^{17}$		$2.161{\cdot}10^{-10}$
p	0.13	2.4	67	$3.6 \cdot 10^{17}$	$6.4 \cdot 10^{-5}$	$1.105{\cdot}10^{-10}$
n	0.18	3.6	758*			$2.9{\cdot}10^{-10}$
p	0.18	3.6	92*		$3.25 \cdot 10^{-5}$	$1.9{\cdot}10^{-10}$
t.o. n (0.18μm)	0.6	13.6	406*			$1.2{\cdot}10^{-10}$
t.o. p (0.18μm)	0.6	13.6	199*	$3.499 \cdot 10^{16}$	$3.25 \cdot 10^{-5}$	$1{\cdot}10^{-12}$

* data from BSIM3v3 model file

Table 6: Technology parameters used in calculations.

Using the EKV model, transistor g_m in saturation is described by

$$g_m = \frac{2I_D}{\eta U_T \left(\sqrt{4ifor+1}+1\right)} \tag{142}$$

capturing the square root reliance on I_D in strong inversion, linear reliance on I_D in weak inversion, as well as a large range of values in moderate inversion where none of these two dependencies are valid.

7.2.1 Thermal Noise Enhancements

Thermal noise factor γ is given by

$$\gamma = \frac{1}{1+ifor}\left(\frac{1}{2}+\frac{2}{3}ifor\right) \tag{143}$$

and equals $\frac{1}{2}$ in weak inversion and $\frac{2}{3}$ in strong inversion.

Transistor gate capacitance C_g is equal to

$$C_g = \frac{1}{\eta}\left(\eta - 1 + c_{GS} + c_{GD}\right) WLC_{ox} + 2C_{OV} \tag{144}$$

where c_{GS} and c_{GD} are normalized intrinsic gate-source and gate-drain capacitance and C_{OV} is the overlap capacitance. To capture the gate capacitance bias dependance in saturation, a simplified equation can be used

$$c_{GS} + c_{GD} = \frac{1}{3}\frac{\left(\frac{1}{2}\sqrt{4ifor+1}-\frac{1}{2}\right)\left(\sqrt{4ifor+1}+2\right)}{\left(\frac{1}{2}\sqrt{4ifor+1}+\frac{1}{2}\right)^2} \tag{145}$$

By plugging in (141)-(145) in (132), the transistor input referred thermal noise

$$V^2_{ngt}(I_D,W,L) = \frac{4kT\eta\gamma(I_D,W,L)}{g_m(I_D,W,L)}\left(\frac{C_m+C_p+C_g(I_D,W,L)}{C_m}\right)^2 \tag{146}$$

can be expressed as a function of I_D, W and L for any region of operation.

From $\frac{dV^2_{ngt}(I_D,W,L)}{dW} = 0$ an optimal W can be calculated as a function of drain current for several transistor lengths. These optimal values are shown in Fig. 36 along with the corresponding thermal noise minima. The plot is for 6V thick oxide pMOS transistor with minimum length $L_{min} = 0.6\mu m$

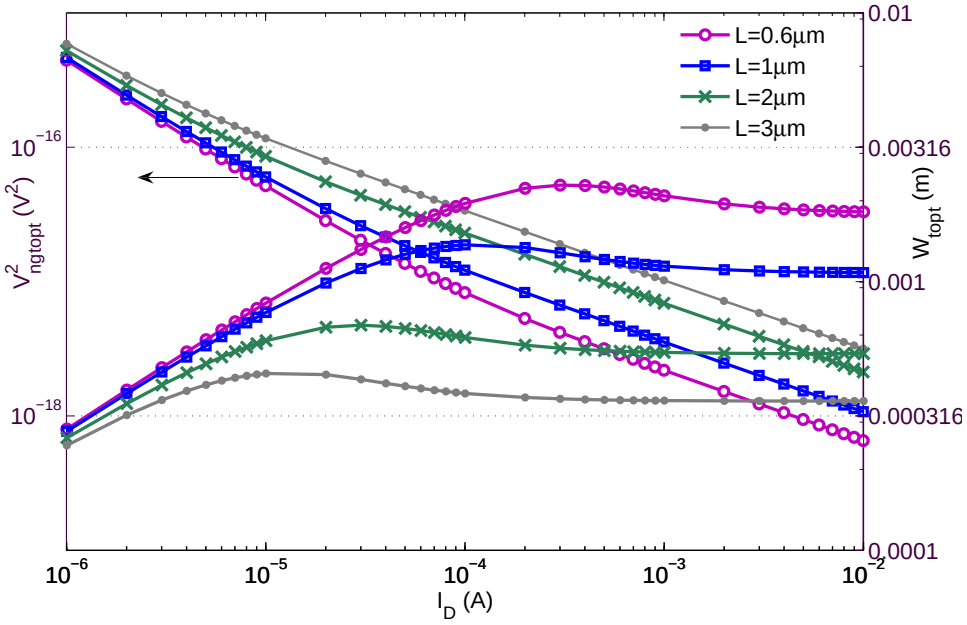


Figure 36: Calculated minimal thermal noise (left scale) and optimal width (right scale) vs. drain current for thick oxide p-type transistors from $0.18\mu m$ CMOS.

from a $0.18\mu m$ CMOS digital technology. Process parameters used for calculations are shown in Table 6.

It can be seen from Fig. 36 that the optimal thermal noise is minimal for minimal transistor length and decreases with the drain current.

In Fig. 37, corresponding transistor capacitance for achieving the optimal thermal noise is shown along with the $ifor$ for the calculated optimal width. Clearly, optimal C_g in strong inversion is equal to (138). A similar analysis is explained in [3], for a charge amplifier, and an analytical formula for the optimal width for thermal noise in moderate inversion is proposed. Proposed analytical formula for the optimal transistor width is

$$W_{topt} = W_{si} \frac{1}{1 + A \cdot \left(\frac{W_{si}}{ifor \cdot W}\right)^m} \tag{147}$$

where W_{si} is a strong inversion optimum and A and m constants found by numerical optimization.

7.2.2 Flicker Noise Enhancements

Flicker, or $1/f$ noise is a dominant noise source in low-frequency analog circuits. Two theories exist about the flicker noise origin: ΔN, number fluctuation theory and $\Delta\mu$, Hooge model or mobility fluctuation theory; more precisely three including $\Delta N - \Delta\mu$ theory as we have seen in the previous chapter. Majority of experimental data up to date show that pMOS transistors follow $\Delta\mu$ theory and nMOS transistors ΔN theory, however in weak inversion often both types follow ΔN theory. Physical parameters used to quantify how 'clean' a technology is concerning the flicker noise are the oxide trap

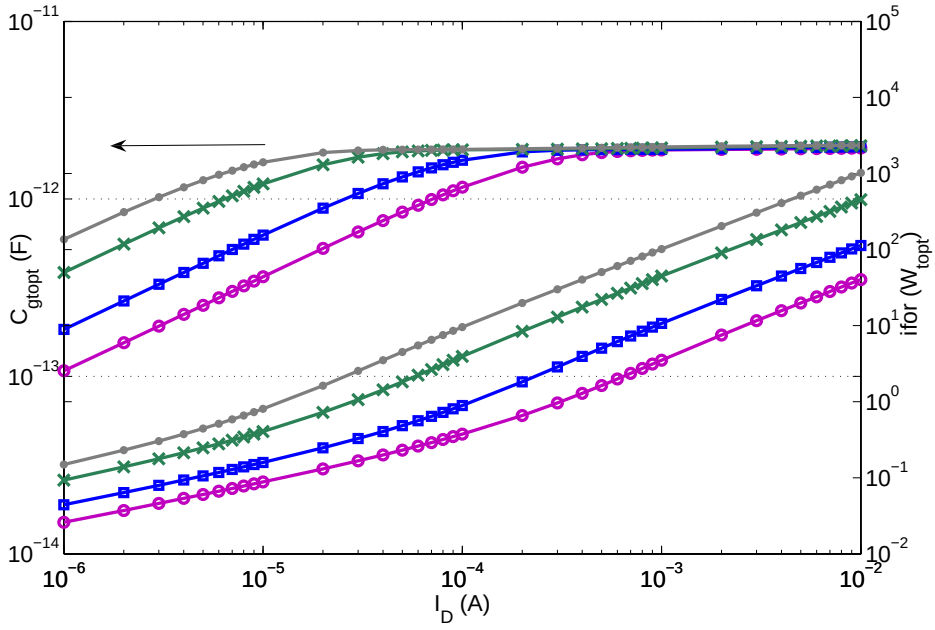


Figure 37: Calculated transistor capacitance for minimal thermal noise (left scale) and $ifor$ for the optimal width (right scale) vs. drain current for thick oxide p-type transistors from $0.18\mu m$ CMOS.

density N_t for ΔN model and Hooge constant α_H for $\Delta\mu$ model. With technology scaling, as the gate oxide thickness is decreasing, a process is more noisy and these parameters are increasing [9].

Circuit designers usually use a simple expression (136) for $1/f$ noise calculation. BSIM3v3 extrapolates flicker noise in moderate inversion using tree fitting parameters which is inconvenient for hand calculations. EKV model formulas valid in all operating regions and describing the two physical noise mechanism have been recently presented. ΔN model is described in [6]-[7] and in $\Delta\mu$ in [6]. The formulas have been used for noise optimization with noise parameters derived from measurement data which are displayed in Table 6. It is assumed in calculations that η is 1.3.

$\Delta\mu$ Flicker Noise Enhancements

From [7], flicker noise of a microphone preamplifier due to mobility fluctuations noise of a transistor working in saturation in weak, moderate or strong inversion can be expressed by

$$V_{ngf\Delta\mu}^2 = \frac{kT\eta\alpha_H}{WLC_{ox}f}\frac{1}{2}\left(1+\sqrt{4ifor+1}\right)\left(1+\frac{2.3\cdot\sqrt{ifor}}{ifor}\right)\times\left(\frac{C_m+C_p+C_g}{C_m}\right)^2 \tag{148}$$

ΔN Flicker Noise Enhancements

On the other hand, ΔN flicker noise is given by

$$V_{ngf\Delta N}^2 = \frac{q^2kTN_t}{WL\gamma C_{ox}^2 f}\left(\frac{1+\sqrt{4ifor+1}}{2}\right)^2\frac{ln(1+4ifor)}{4ifor}\times\left(\frac{C_m+C_p+C_g}{C_m}\right)^2 \tag{149}$$

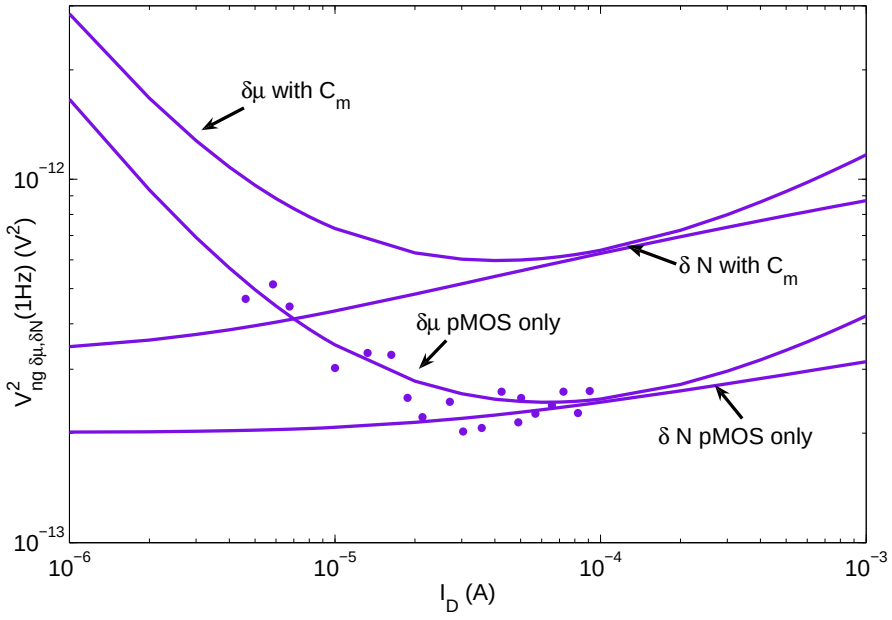


Figure 38: Flicker noise calculations and measurements for thick oxide pMOS with W=600μm, L=3μm.

where γ is the tunneling constant of the traps ($10^8/cm$) and q electron charge.

The difference between the two models can be seen in Fig. 38; flicker noise PSD at 1Hz is displayed as a function of drain current when calculated by using (148) and (149) for an amplifier loaded with a microphone with C_m=5.6pF and C_p=0.5pF. In the same figure, PSD at 1Hz is plotted as a function of drain current when calculated for the transistor only if $\Delta\mu$ model applies as well as if ΔN model applies. As explained in literature, flicker noise dependence on bias is more pronounced for mobility fluctuations model than for number fluctuations model; for number fluctuations model, noise is almost constant, while for mobility fluctuations, it is minimal in the moderate inversion region. Calculations are done for a thick oxide pMOS transistor with W=600μm and L=3μm with parameters from Table 6 and measurement results for the same transistor are plotted (dots) along with calculations in Fig. 38. The measurements are done on the amplifier explained in the next part of this thesis. From Fig. 38 it can be clearly seen that thick oxide pMOS measured follow mobility fluctuation model for the technology used.

Solution for the $\frac{dV^2_{ngf\Delta\mu}(I_D,W,L,1Hz)}{dW} = 0$ is shown in Fig. 39 as a function of drain current for several transistor lengths (thick oxide transistors). The minimal noise for that optimal W is shown in the same figure and the inversion coefficient $if or$ for that optimal W in Fig. 40 along with the calculated gate capacitance for the optimal width. It can be also seen that the minimal $\Delta\mu$ flicker noise is obtained when the transistor is working in moderate inversion with an inversion coefficient $if or$ close to two. It can be seen that the noise minimum is equal independent of the transistor length and it is beneficial to use an L greater than the minimum as the same minimum noise can be achieved with less current. In the same figure it can bee seen that for high currents, when a transistor is working in strong

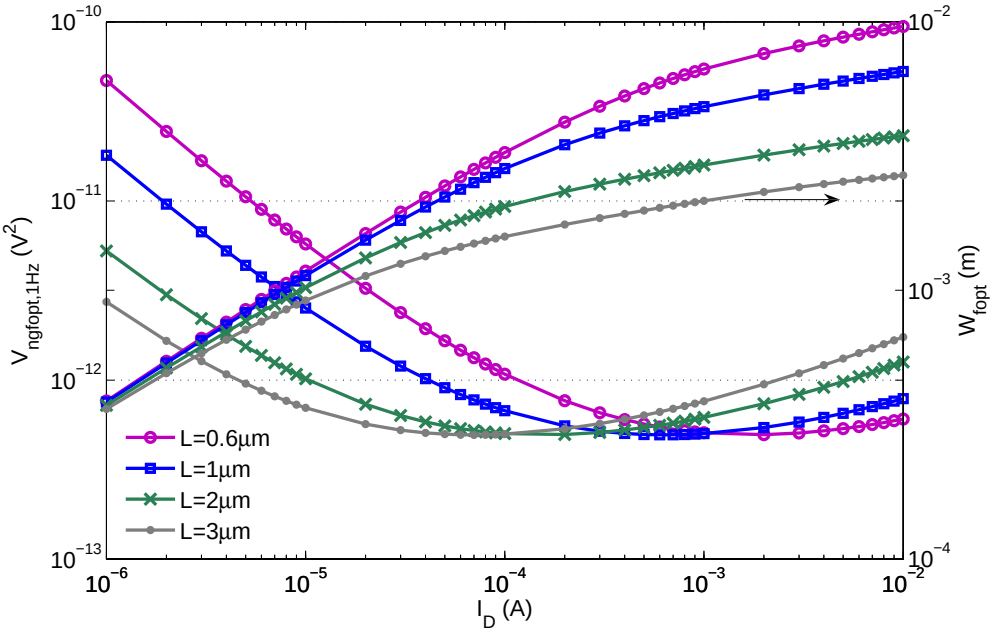


Figure 39: Calculated minimal $\Delta\mu$ flicker noise (left scale) and optimal width (right scale) vs. drain current for thick oxide p-type transistors from $0.18\mu m$ CMOS.

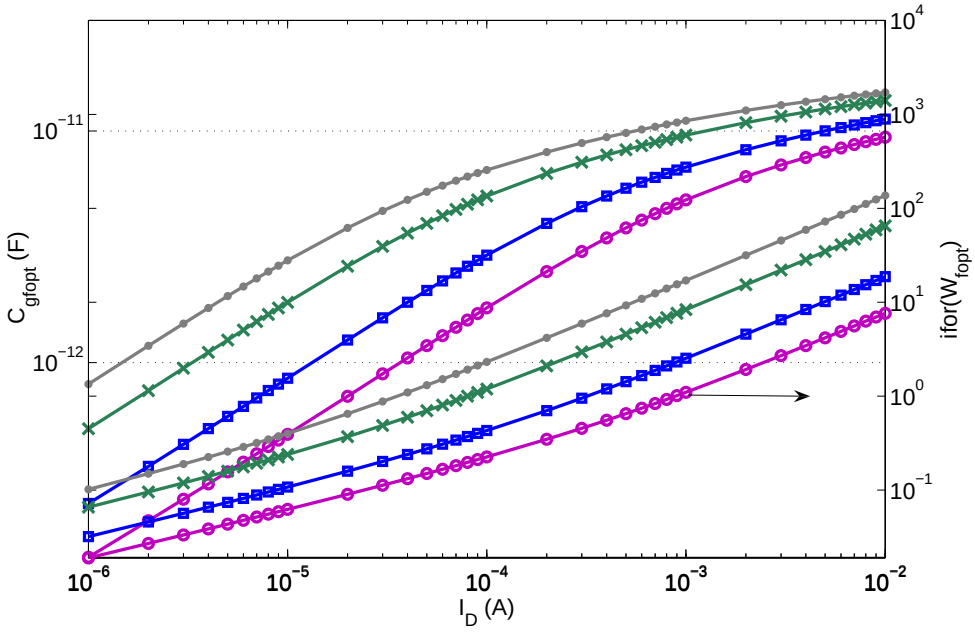


Figure 40: Calculated optimal transistor capacitance for minimal $\Delta\mu$ flicker noise (left scale) and $ifor$ for the optimal width (right scale) vs. drain current for thick oxide p-type transistors from $0.18\mu m$ CMOS.

inversion, for the same drain current noise optimum is increasing with increased transistor length. On the other hand, for low currents when a transistor is working in weak inversion, noise optimum

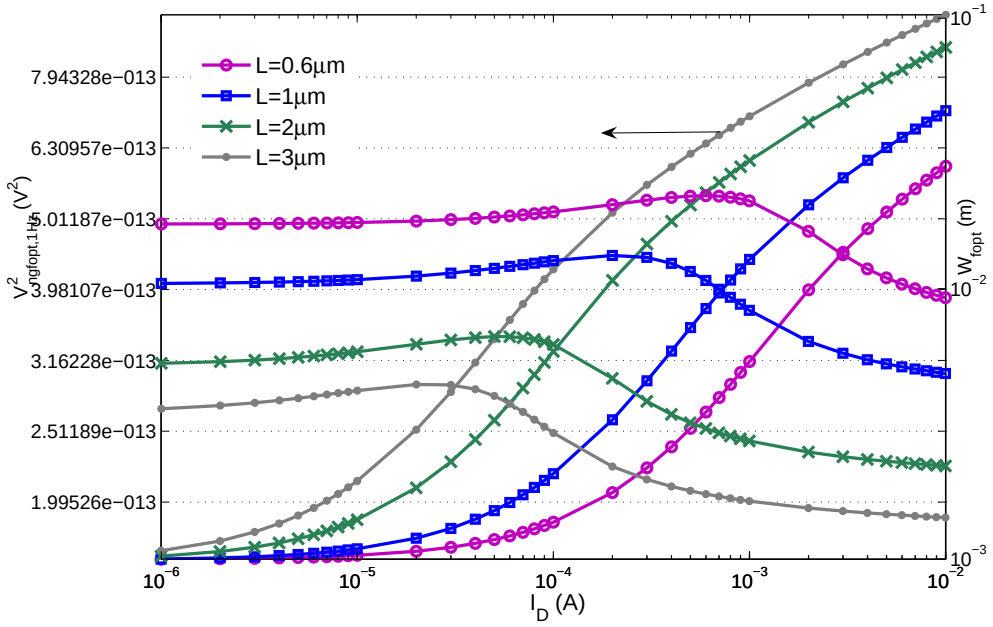


Figure 41: Calculated minimal ΔN flicker noise (left scale) and optimal width (right scale) vs. drain current for thick oxide p-type transistors from $0.18\mu m$ CMOS.

is less for a longer transistor. By curve fitting of the optimal width curve for a transistor working in moderate inversion plotted in Fig. 39 an analytical solution for W_{opt} can be found. Using hand calculations, it is possible to find a derivative of (148) with resect to WL for $ifor$=2. For $ifor = 2$, $C_g \approx 0.55WLC_{ox} + 2C_{ov} = \alpha WLC_{ox}$, where notation with a proportionality constant α is introduced to simplify the analysis. It can be shown that the minimum noise is achieved for $C_m + C_p = WLC_{ox}\alpha$ and the minimal noise would then be

$$V^2_{ngf\Delta\mu,min} = \frac{4\alpha kT\eta\alpha_H}{f}(2 + 2.3\sqrt{2})\frac{C_m + C_p}{C_m^2} \tag{150}$$

It can be noticed that the minimum depends only on the noise parameter α_H. The minimum is achieved for an optimal transistor area and for greater transistor lengths and less W, $ifor = 2$ is obtained at lower currents.

Solution for the $\frac{dV^2_{ngf\Delta N}(I_D,W,L,1Hz)}{dW} = 0$ is shown in Fig. 41 as a function of drain current for several transistor lengths. The minimal noise for that optimal W is shown in the same figure and the inversion coefficient $ifor$ for that optimal W in Fig. 42 along with the gate capacitance for the optimal width. From Fig. 41 it can be seen that the optimal ΔN flicker noise is minimal for a transistor in weak inversion and with minimal length.

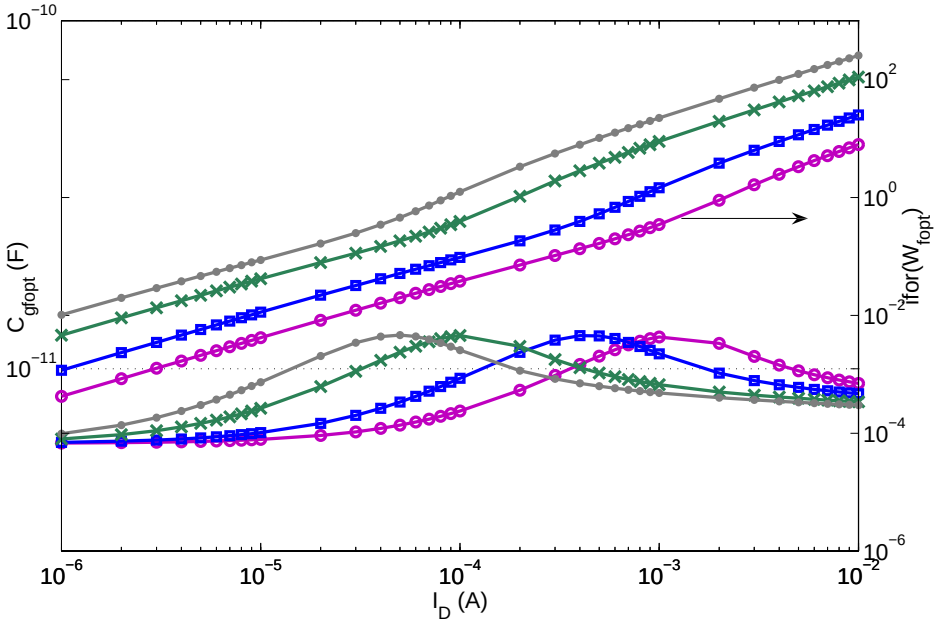


Figure 42: Calculated optimal transistor capacitance for minimal ΔN flicker noise (left scale) and $ifor$ for the optimal width (right scale) vs. drain current for thick oxide p-type transistors from $0.18\mu m$ CMOS.

7.3 Preamplifier Total Noise Optimization

The SNR of the microphone with the amplifier is calculated as the microphone signal V_m for sound pressure level of one Pascal divided by the A-weighted integrated (20Hz-20kHz) input referred noise or

$$SNR = 20 \cdot \log \left(\frac{V_m}{\sqrt{\int_{20Hz}^{20kHz} A^2(f) \cdot V_{ni}^2(f) df}} \right) \tag{151}$$

where the standard A-weighting filter function typically used is

$$A(f) = \frac{1.87192 \cdot 10^8 f^4}{(f^2 + 20.6^2)(f^2 + 12200^2)\sqrt{f^2 + 107.7^2}\sqrt{f^2 + 738^2}} \tag{152}$$

An amplifier output noise spectrum with and without A-weighting filter is shown in Fig. 43. A-weighting filter follows the sensitivity of a human ear.

Neglecting the microphone own noise, the total A-weighted rms input noise consisting of transistor flicker noise, transistor thermal noise and bias resistor noise can be calculated as

$$V_{ni,A-W,rms}^2 = \int_{20Hz}^{20kHz} \frac{A^2(f)}{f} \cdot V_{ngf}^2(1Hz) df + \int_{20Hz}^{20kHz} A^2(f) \cdot V_{ngt}^2 df + \frac{4kTf_p}{C_m 2\pi} \int_{20Hz}^{20kHz} \frac{A^2(f)}{f^2} df \tag{153}$$

with f_p being the lower cut-off frequency of the transfer function from the microphone to the amplifier output ($f_p = \frac{1}{2\pi C_m R_b}$). The noise contribution due to the amplifier output resistance is neglected. If A-weighting factor for each contribution is calculated, we obtain

$$V_{ni,A-W,rms}^2 = 3.57 \cdot V_{ngf}^2(1Hz) + 12448.6 \cdot V_{ngt}^2 + \frac{4kTf_p}{C_m 2\pi} \cdot 0.00263 \tag{154}$$

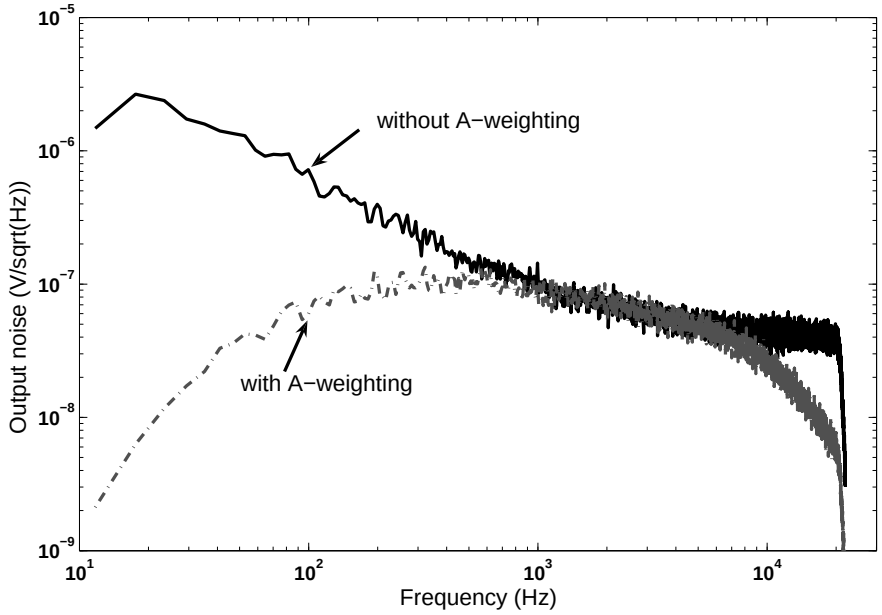


Figure 43: An amplifier output noise with and without A-weighting filter.

Without A-weighting, integrated (20Hz-20kHz) thermal noise squared from (154) should be multiplied with 1.6 times greater coefficient and flicker noise squared at 1Hz with 1.93 times greater coefficient.

7.3.1 Technology Comparison

Noise optimization for a capacitive microphone is studied for pMOS transistors for three cases: thick oxide transistors with minimum length $0.6\mu m$ from a $0.18\mu m$ CMOS process, thin oxide transistors from the same technology ($0.18\mu m$ CMOS) and transistors from a $0.13\mu m$ CMOS process. Parameters used in calculations are displayed in Table 6. Values of N_t and α_H for thick oxide transistors and for transistors from $0.13\mu m$ process are extracted from noise measurement data. It is assumed in calculations that the noise parameters for $0.18\mu m$ thin oxide transistors are the same as for the thick oxide transistors from the same technology. Usually flicker noise of the thin oxide transistors is slightly higher than the noise of the thick oxide transistors from the same technology [11]-[13]. Measurement results show that for p-MOS transistors used here from $0.18\mu m$ CMOS (both thick and thin oxide), flicker noise follow $\Delta\mu$ noise theory. $1/f$ noise of p-MOS from $0.13\mu m$ process is ΔN in weak inversion and $\Delta\mu$ otherwise. Microphone capacitance is 5.6pF and parasitic capacitance 0.5pF.

Choice of the Overall Optimal Device

Minimal total transistor noise calculated using (154) for the thick oxide transistors is shown in Fig. 44 for several transistor lengths and drain currents along with the optimal width for which the noise minimum is obtained. Calculations are done using $\Delta\mu$ model, and it can be seen that for L less than $3\mu m$ optimal drain current I_D and transistor width W_{opt} are very close to the optimum

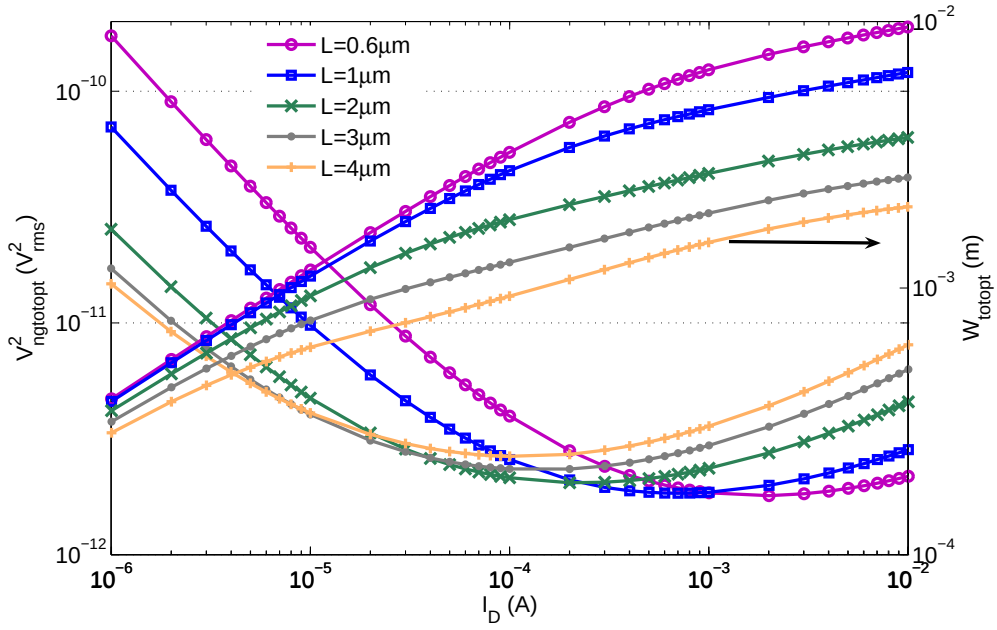


Figure 44: Calculated minimal total noise (left scale) and optimal width (right scale) vs. drain current for thick oxide p-type transistors from 0.18μm CMOS.

calculated for flicker noise only shown in Fig. 39, i.e. $ifor$ for the minimal noise is close to 2 and the noise minimum is independent of the transistor length. With increased transistor length, thermal noise increases and the total noise minimum is achieved for somewhat larger currents than the flicker noise minimum; for $L = 4\mu m$ the total noise minimum is achieved at $ifor$ around 5. The minimal rms noise that can be obtained with this technology is $1.8 \cdot 10^{-12} V^2_{rms}$ with minimal L and I_D 2mA. If $L = 2\mu m$ is used, a minimum of $2 \cdot 10^{-12} V^2_{rms}$ is obtained for $200\mu A$.

In Fig. 45 calculations of the minimal total A-weighted integrated noise versus drain current are shown for thin oxide transistors from 0.18μm CMOS process for several transistor lengths. Optimal transistor width is shown in the same figure. The same noise parameter as for thick oxide transistors is used for noise calculations. For the dimensions plotted, thermal noise is not significant and the optimum conditions are equal to the flicker noise optimum which is achieved for $ifor$ around 2. The noise optimum is independent on the transistor length and for lower current consumption, a non-minimal transistor length should be used. The thermal noise becomes noticeable and the total noise minimum increases for L between $1\mu m$ and $2\mu m$. From the figures, it can be seen that the minimal rms noise that can be obtained by using thin oxide transistors from this technology is almost the same as when using thick oxide transistors from the same process for relatively small transistor lengths; this is because flicker noise is dominant, α_H factor same for both types of transistors and flicker noise optimum doesn't depend on C_{ox}. Using a higher α_H for thin oxide than thin oxide transistors, thick oxide show better noise performance. As a comparison, if ΔN model was valid with the same N_t for both thick and thin oxide transistors, less minimum $1/f$ noise would be achieved with thin oxide transistors from 0.18μm CMOS than thick oxide transistor from 0.18μm CMOS as the noise optimum

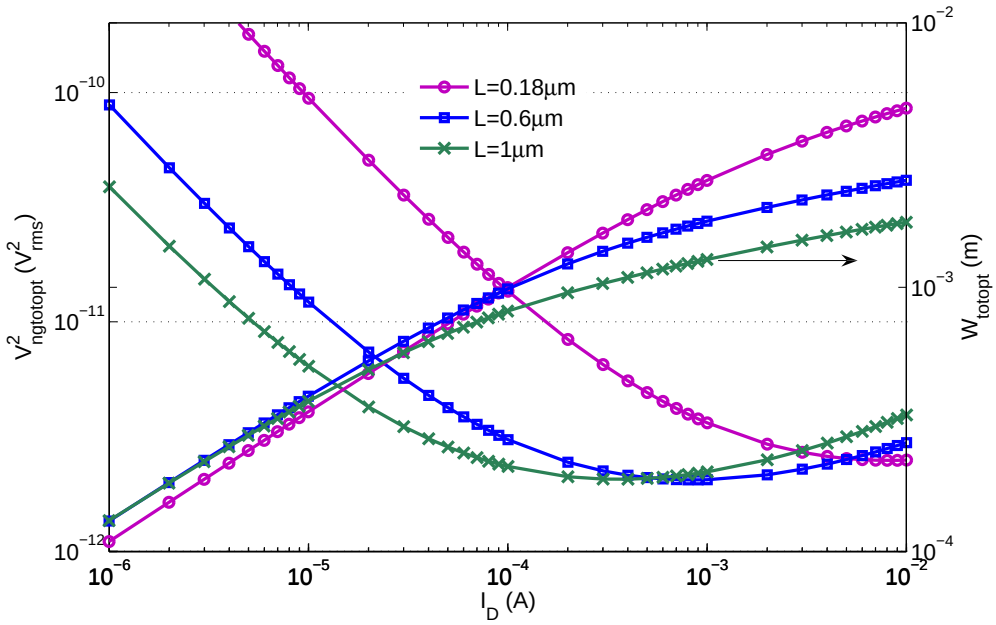
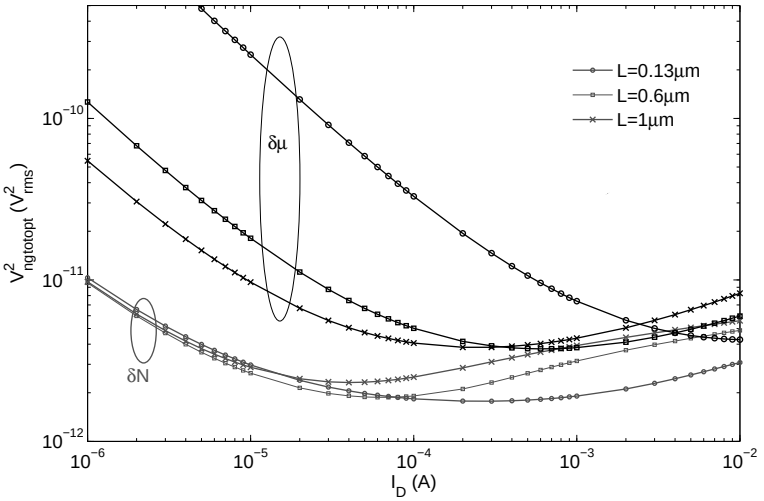


Figure 45: Calculated minimal total noise (left scale) and optimal width (right scale) vs. drain current for p-type transistors from 0.18μm CMOS.

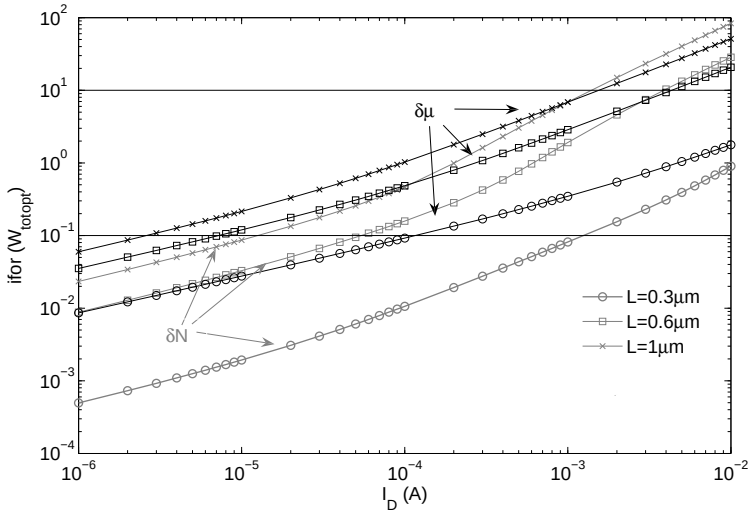
for this case would be proportional to N_t/C_{ox}.

In Fig. 46(a), calculations of the total minimal A-weighted rms noise versus drain current are shown for transistors from a 0.13μm CMOS process for several transistor lengths if $\Delta\mu$ model is used as well as if ΔN model is used for flicker noise. As shown in Fig. 41, using ΔN model minimal flicker noise increases with drain current and is minimal, almost constant, in weak inversion and minimal for minimal transistor length. However, reducing the drain current leads to increased thermal noise and therefore the total noise minimum in Fig. 46(a) is in weak inversion at a point where the thermal noise is not significant. The noise minimum shown in the same figure increases with transistor length and for L less or equal 0.6μm, the optimum is in weak inversion, i.e. $ifor$ calculated for the width that the noise minimum is obtained with is less than 0.1. With L=0.13μm a noise minimum of $1.8 \cdot 10^{-12} V^2_{rms}$ is obtained for 300μA and W_{opt}=9mm. If L=0.6μm is used and at 60μA, noise minimum will be slightly higher. In Fig. 46(c), the optimal corresponding to the minimal noise from Fig. 46(a) is shown and in Fig. 46(b), the corresponding inversion coefficient is displayed. As the pMOS transistors from this process have flicker noise due to both mechanisms, optimization using $\Delta\mu$ model is shown in Fig. 46(a) as well. Using the $\Delta\mu$ model, the total noise optimum is for conditions when $ifor$ is close to 2, where the flicker noise optimum is. In saturation, when this model is valid the optimal noise increases with transistor length.

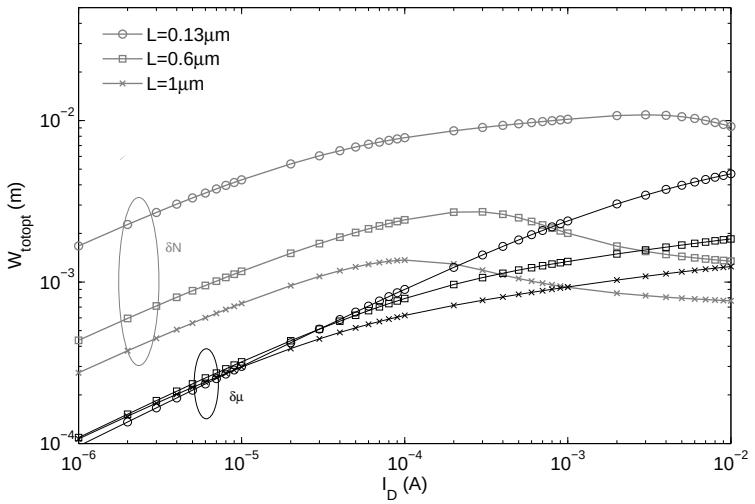
This analysis presented shows that even though the 0.13μm process is more noisy than 0.18μm process, using it and biasing a transistor in weak inversion, a good noise performance can be achieved. Another observation is that for all the cases described, optimal performance with the microphone used is achieved in moderate/weak inversion and a simple analysis for a strong inversion case is insufficient.



(a) Calculated minimal total noise vs. drain current



(b) Inversion coefficient for optimal transistor width



(c) Calculated optimal width vs. drain current

Figure 46: Noise optimization for p-type transistors from $0.13\mu m$ CMOS.

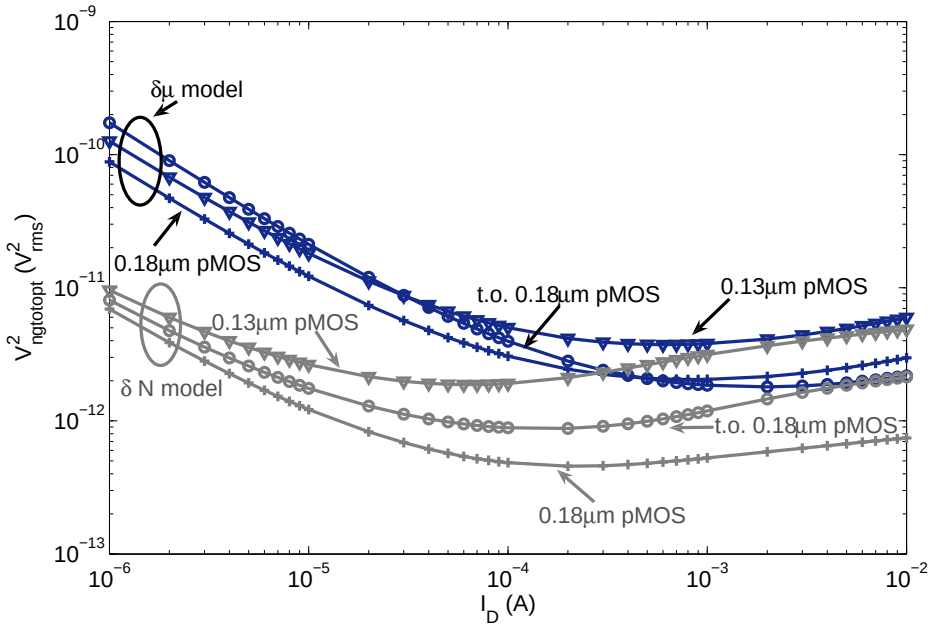


Figure 47: Calculated minimal total noise for pMOS for three technologies, with the same length L=0.6μm.

7.3.2 Bias Resistor Influence

Integrated A-weighted noise of the bias resistor R_b can be calculated as

$$\frac{kT}{\pi^2 C_m^2 R_b}\int_{20Hz}^{20kHz}\frac{A^2(f)}{f^2}df = \frac{kT}{\pi^2 C_m^2 R_b}\cdot 0.00263 \tag{155}$$

With C_m=5.6pF, noise contribution for several values of the bias resistor can be calculated and R_b can be chosen that doesn't contribute to the total noise significantly. More precisely R_b can be calculated using

$$\frac{kT}{\pi^2 C_m^2 R_b}\int_{20Hz}^{\frac{kT}{\pi^2 C_m^2 R_b V_{ngf}^2(1Hz)}}\frac{A^2(f)}{f^2}df \tag{156}$$

where $V_{ngf}^2(1Hz)$ is flicker noise at one Hertz. As an example, using Fig. 46(a) and Fig. 39 total noise for thick oxide transistors with L=0.6μm has a minimal value of $1.87\cdot 10^{-12}V_{rms}^2$ and flicker noise at 1Hz which is also minimal for this case equal to $4.97\cdot 10^{-13}V_{rms}^2$. Replacing that value of flicker noise at 1Hz in (156), it can be calculated that the bias resistor noise is 10% of the minimal transistor noise for R_b=57$G\Omega$ i.e. for pole frequency 0.5Hz.

8 Conclusion III

Thermal noise optimization for capacitive sources has been revisited. Flicker noise formulas valid in all regions and using physic based noise models have been applied for optimization of a microphone preamplifier. The computation show that $\Delta\mu$ flicker noise of the preamplifier with the microphone is minimal for moderate inversion operation of the input transistor and the minimum is reached for

$if or$ close to 2. Total noise optimization with A-weighting filter has been done for three types of devices with noise parameters extracted from measurement data. The analysis performed gives design guidelines for obtaining an optimal noise performance of a transistor interfacing a capacitive source. It has also been verified that choosing a minimal transistor length is not always an optimal design choice re. minimal current consumption. Calculations with the physical parameters presented give an insight into technological noise limits for a process, and are a tool applicable to other technologies as well. Comparing to a commercially available BSIM3v3 circuit simulator model, using three fitting parameters for flicker noise model, the EKV model used in the calculations is much more convenient for hand calculations and computer-based analysis. Maple files used for calculations here can be used as an in-house simulator for the optimization of preamplifiers with a capacitive source based on physical noise parameters. At the moment, no simulator can be found using the formulas presented.

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9 Preamplifier for Two Microphones

9.1 Increasing the SNR by Using Two Microphones

One of the key parameters of a microphone is its equivalent input noise. It is calculated in dB(A) SPL where dB is relative to sound pressure level (SPL) of $20\mu Pa$ and A refers to A-weighting filter function used for weighting the noise power spectrum. Conventional microphones with a larger membrane radius have lower noise. The same applies for micromechanical microphones which noise even usually dominates the noise of the accompanying electronic circuit. An equivalent input pressure noise of the microphone is generated by the flow of separate air molecules intruding the microphone diaphragm (the Brownian motion).

Analogous to thermal noise in electrical circuits, acoustical noise is generated by dissipative mechanisms in connection with propagation of sound i.e. the acoustic resistances. Thermal noise of the MEMS microphone can be calculated as [1]

$$V_{n,mic}^2 = \frac{8\sigma tkT}{\pi R^4} \tag{157}$$

where σ is the membrane mechanical stress, t membrane thickness, R membrane radius, k Boltzmann constant and T temperature.

Another important microphone property is its sensitivity i.e. change in capacitance with sound pressure, which increases with increased membrane radius and decreases for greater membrane areal density (mass per unit area). Microphone own SNR (microphone output signal for 1Pa, 1kHz input sound pressure divided by the microphone rms noise in 20-20kHz band with or without A-weighting filter) is thus an intrinsic microphone property and is in first approximation independent of the microphone bias.

Even though microphones with a larger membrane have a higher SNR, to be competitive on the microphone market where the price is set by the cheap traditional electret condenser microphones (ECM), a MEMS microphone die size is minimized to reduce cost. MEMS microphone die with an SNR 63dB-66dB, depending on the process details, is used here.

As explained in the chapter dealing with microphone basics, the design of MEMS microphones is a challenging task with a number of tradeoffs [1]-[2] and redesigning a microphone die is certainly not trivial. In this work, we demonstrate a method to increase a MEMS microphone SNR by using two 'unity size' MEMS dies in a differential configuration.

The key idea behind the principle is that the two microphones biased with voltages of opposite polarities V_b and $-V_b$ produce signals of opposite polarities when a sound pressure is applied [3] (Sonion/Pulse's patent pending). The illustration of the principle is shown in Fig. 48 where the microphones are represented by their capacitance C_m in series with the microphone output signal V_m. If these two microphones are connected to a differential amplifier a 3dB higher SNR can be achieved comparing to a single microphone solution; or an SNR maximally 3dB higher than the own intrinsic microphone SNR can be achieved if the following preamplifier doesn't contribute to noise, as shown by the formula

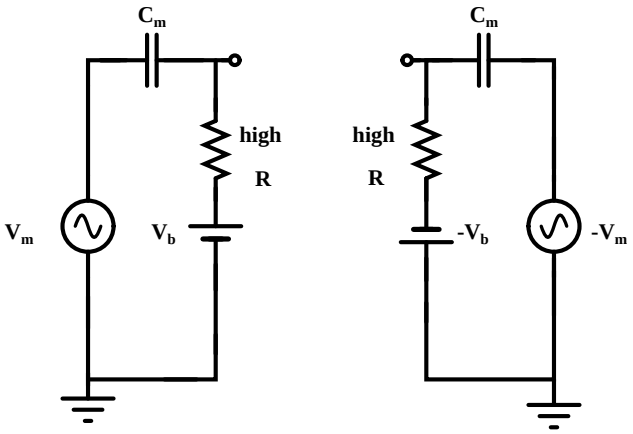


Figure 48: Two microphones with opposite polarity bias produce differential signals.

$$SNR = 20 \cdot log \frac{2V_m}{\sqrt{2V_{n,mic}^2 + V_{nin,amp,rms}^2}} \tag{158}$$

where V_m is the microphone signal, $V_{n,mic}$ microphone noise and $V_{nin,amp,rms}$ integrated amplifier input noise. In this way, an SNR improvement equivalent to using a microphone with a larger membrane area can be achieved by only designing suitable electronics without any complicated and risky MEMS microphone redesign.

In this PhD work, a novel preamplifier capable of handling the signals from the two microphones has been designed. Using a compact packaging method employed in Pulse's products, all silicon chip scale package (CSP) consisting of the two MEMS microphone dies and the amplifier die has been assembled. In the following text, the design of the implemented microphone preamplifier will be described followed by the description of the implemented CSP and the discussion of the measurement results on the CSP. Basic building blocks of the amplifier including a charge pump for microphone biasing will be described.

9.2 Preamplifier Description

A simplified schematic of the preamplifier for the two microphones designed is shown in Fig. 49. The basic gain stage is formed by the pMOS differential pair (transistors M_1 and M_2) loaded with the resistors R_1 and R_2. Preamplifier gain is 8dB. C_c are DC blocking capacitors, decoupling the MOS gates from the input bias voltages and are chosen to be much larger than the microphone capacitance C_m. A high output impedance is needed to isolate the microphones and the charge pumps delivering the microphone bias voltages V_b and $-V_b$ and it is provided by the diode pairs $D_{p1,p2}$ and $D_{p3,p4}$ connected in a back-to-back (cross-coupled) configuration. Polysilicon diodes, which will be described in the later text, have no contact with the substrate and are used to ensure that the leakage currents and latch-up hazards due to the microphone bias voltages are avoided.

DC paths from the gates of the input transistors M_1 and M_2 and ground are provided by the two more sets of diodes in a back-to-back configuration: D_1-D_2 and D_3-D_4 implemented as $n^+ - pwell$ junctions inside a deep n-well. A resistance presented by these diodes changes as a function of time and

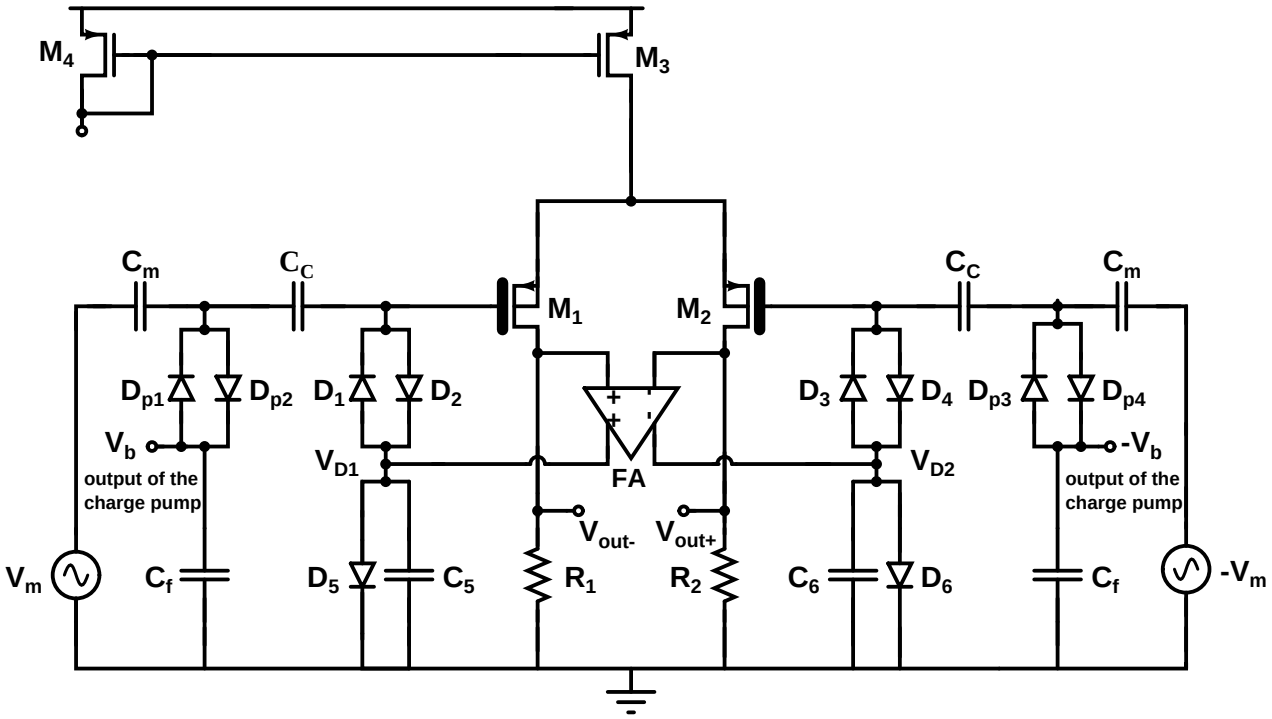


Figure 49: Preamplifier for two microphones.

is very high at zero current. As the diode resistance changes, the lower cut off frequency, $\approx \frac{1}{2\pi C_m R_{diodes}}$, of the transfer function from the microphones to the differential output (V_{out+}-V_{out-}) changes and is well below 20Hz for zero current over diodes.

Except for ensuring a flat frequency response in the 20Hz-20kHz band, this high resistance is needed for low noise as well. As the resistance of the diodes changes as a function of time, their noise contribution changes as well and is negligible after 3 seconds.

9.2.1 Preamplifier Design Basics

A signal from a microphone has traditionally been amplified by a JFET source follower, which has been replaced by a single MOS transistor with the advance of MOS technology.

A single pMOS transistor in a common-source configuration interfacing a microphone is shown in Fig. 34 in the chapter on noise optimization for capacitive sources. A common-source configuration is chosen as it is known that the source-follower (common-drain) introduces equal amount of noise to the input signal as the common-source amplifier without providing any gain (its gain is less than unity). Therefore, source-follower is usually avoided in low-noise designs [4]. Further more, as pMOS transistors usually have less noise than nMOS, they are preferred as the input transistor and are chosen here.

In some microphone amplifier solutions a differential amplifier is used (for example [5]-[6]) for amplification of a signal from a single (electret) microphone. Using a differential amplifier has numerous advantages over a single transistor amplifier solution such as common-mode noise rejection, insensitivity

to supply noise, larger maximum achievable voltage swing, higher linearity and simpler biasing. A minor disadvantage of the differential configuration comparing to a single-ended one is the area penalty.

It can be calculated that the gain of a common-source amplifier (from its gate to the drain) is $-g_m R_{out}$ where g_m is the amplifier input transistor transconductance and R_{out} the resistance seen at the transistor drain equal load resistance R_D in parallel with the transistor drain-source resistance r_{ds}, $R_{out} = R_D \parallel r_{ds}$.

If a differential amplifier has the input transistors having the same transconductance as the common-source amplifier (meaning that the tail current of the differential pair is two times larger than the current of the common-source amplifier), its differential gain will be the same as for the common-source stage. So the differential gain from the gates of a differential pair to its outputs is

$$\left| \frac{V_{out+} - V_{out-}}{V_{in+} - V_{in-}} \right| = g_m \left(R_D \parallel r_{ds} \right) \tag{159}$$

When a common-source single transistor amplifier or a differential amplifier are used as an interface to a microphone (Fig. 34 chapter on noise optimization and Fig. 49 this chapter), the transfer function from the microphone to the amplifier output will have a high-pass behavior and it is possible to write

$$H(s) = \frac{V_{out+} - V_{out-}}{V_{m+} - V_{m-}} = -g_m R_{out} \frac{C_m}{C_m + C_p + C_g} \frac{s}{s + \frac{1}{R_b (C_m + C_p + C_g)}} \tag{160}$$

where V_m is the microphone signal, C_m microphone capacitance, C_p capacitance seen from the input transistor gate to ground, C_g the input transistor gate capacitance and R_b resistance at the input transistor gate. It is assumed that the coupling capacitance C_c is much larger than the microphone capacitance and that the C_m only is seen at the input transistor gate.

In a properly designed microphone front end, its frequency response should be flat in the audio band (20Hz-20kHz) and the gain is

$$A_v = g_m R_{out} \frac{C_m}{C_m + C_p + C_g} \tag{161}$$

The lower cut-off frequency of the transfer function is equal to

$$\omega_{3dB} = \frac{1}{R_b \left(C_m + C_p + C_g \right)} \tag{162}$$

In some applications the lower cut-off frequency should be below 100Hz only, in our application the microphone response cut-off is 20Hz and the amplifier should be designed for having a lower cut-off frequency than the microphone. It is easy to show, that the output noise per unit bandwidth of a differential pair microphone preamplifier can be calculated as

$$V^2_{nout,amp}(f) = 2R^2_{out} I_{nR_{out}}(f)^2 + 2R^2_{out} I_{Dn}(f)^2 + 2(g_m R_{out})^2 \frac{R_b^2}{\left| 1 + j\omega R_b \left(C_p + C_g + C_m \right) \right|^2} I^2_{nR_b}(f) \tag{163}$$

where $I_{nR_{out}}(f)$ is thermal noise power spectral density of the output resistor, $I_{Dn}(f)$ input transistor drain current noise power spectral density (PSD) and $I_{nR_b}(f)$ bias resistor thermal noise PSD. Clearly, the input referred noise can be obtained by dividing (163) with the gain (161).

Output noise squared when using a common-source single transistor amplifier is half this value for the same voltage gain, i.e. for two times less circuit current consumption, what is the only advantage of a singe transistor configuration comparing to a differential amplifier.

Depending on the required signal-to-noise-ratio (SNR) which is calculated as

$$SNR = \frac{C_1 A_v V_m}{\sqrt{C_2 A_v^2 V_{n,mic}^2 + C_3 V_{nout,amp,rms}^2}} \tag{164}$$

where $V_{n,mic}$ is microphone noise, V_m microphone signal and $V_{nout,amp,rms}$ integrated amplifier output noise from (163), one of the three topologies can be chosen; 1) a single transistor common-source topology ($C_1 = 1$, $C_2 = 1$ and $C_3 = \frac{1}{2}$), giving better SNR than 2) a differential pair with one microphone ($C_1 = 1$, $C_2 = 1$ and $C_3 = 1$) as its noise is two times larger than the noise of a common-source amplifier squared; and 3) a topology presented here using two microphones and thus doubling the microphone signal and a differential amplifier ($C_1 = 2$, $C_2 = 2$ and $C_3 = 1$).

The third method presented here has all the advantages of a differential configuration and a superior SNR performance comparing to the other two topologies. To improve linearity (minimize total harmonic distortion), a source resistance is needed in a common-source amplifier configuration and this configuration requires a supply voltage regulator in practical implementations.

9.2.2 Preamplifier Design Constraints

The design tradeoffs of the differential pair amplifying the signal V_m from the two microphones shown in Fig. 49 will be explained. The amplifier supply voltage is 1.8V and its current consumption has to be as low as possible. In the introduction chapter of this thesis specifications for a microphone (with amplifier) for hearing instruments applications are shown in Table 1.

As the signal-to-noise ratio of MEMS microphones is relatively low comparing to high-quality electret microphones, one of the key issues in the design of a MEMS microphone preamplifier is its noise performance. The sensitivity of the MEMS microphone used here is $4.2\frac{mV_{rms}}{Pa}$ and its A-weighted rms noise $V_{n,mic}$=$2.5\mu V_{rms}$ at microphone bias voltage $V_b = 10V$. This gives own microphone SNR equal 64.5dB. Using (164) it can be seen that if the amplifier noise is zero, we can achieve maximum 67.5dB using two microphones with differential signals. If the input referred A-weighted rms noise of the differential amplifier $V_{nin,amp,rms}$ is $2\mu V_{rms}$, the SNR can be calculated to be 66.3dB, i.e. 1.2dB below the maximum achievable value. We aim at designing the preamplifier that will not influence the overall noise more than this.

Noise measurement results available prior to this design have revealed that the pMOS transistors used follow $\Delta\mu$ theory and they have revealed that the thick oxide transistors have a lower noise parameter α_H than the thick oxide transistors from the same technology. For noise optimization, results presented in the chapter on noise optimization are used. Minimum obtainable noise using thick and thin oxide transistors when $\Delta\mu$ noise is valid have been compared in Fig. 44 with Fig. 45 in the chapter on noise optimization and it has been shown that if α_H is lower for thick oxide transistors, less minimum noise can be achieved which is the reason to use them here. It has been shown that when flicker noise is the dominant part, minimum total noise is obtained by biasing transistor in moderate

inversion close to inversion coefficient $ifor$ equal 2. Further more, it has been shown that as long as flicker noise is dominant (for $\Delta\mu$ noise), increasing transistor length means that the same noise optimum can be achieved using less current.

If the transistor current consumption is limited to $50\mu A$, from calculations results shown in Fig. 44, L=$3\mu m$ is chosen. Using the same figure, it can be seen that the corresponding optimal width is W=$1000\mu m$ and that the rms noise squared is $2.5\mu V^2$, giving $\sqrt{2}\sqrt{2.5\mu V^2} = 2.23\mu V$ when using two transistors in a differential amplifier. This is somewhat larger than the specified $2\mu V$. In the calculations in the noise optimization chapter, the total noise is overestimated due to integrations in the whole audio band, it can be shown that integrating the thermal noise from the corner frequency to 20kHz would give less total noise, therefore we continue analysis with the previously chosen dimensions. Calculating the inversion coefficient ($ifor = \frac{I_D L}{2\eta U_T^2 \mu C_{ox} W}$) with parameters from Table 6, it can be confirmed that it is close to 2. As the total noise minimum for the chosen dimension is obtained at the point where flicker noise is minimal, the transistor gate capacitance C_g for the optimal $W \cdot L$ is close to $C_m + C_p$ as explained.

The next parameter to be considered is the amplifier gain. Nowadays microphones typically have a sensitivity between -20 and -40dBV@1Pa, 1kHz. We have chosen to design a system which will give around $10mV_{rms}$ out for 1Pa sound pressure level, single ended output, i.e. have sensitivity around -33.9dBV@1Pa, 1kHz. With a microphone having own sensitivity $4.2\frac{mV_{rms}}{Pa}$ this means that the differential gain of the amplifier should be around 2.4, i.e. close to 8dB.

Transistor g_m in the mid band gain formula (161) can be expressed as a function of drain current and inversion coefficient using EKV model and we get

$$A_v = \frac{2I_D}{\eta U_T \left(\sqrt{4ifor + 1} + 1\right)} R_{out} \frac{C_m}{C_m + C_p + C_g} \tag{165}$$

We have seen that for optimum transistor noise $ifor = 2$ and $C_g = C_m + C_p$; we assumed microphone capacitance C_m to be 5.6pF and C_p=0.5pF, giving $\frac{C_m+C_p+C_g}{C_m} = 2.2$ and as we have chosen to limit the current consumption to $50\mu A$, we can calculate that under these conditions for gain 2.5, R_{out} should be around $7k\Omega$. A transistor output conductance $g_{ds} = \frac{I_D}{LV_a}$ where V_a is Early voltage is typically much larger than this value.

It is required not to have the output resistance which contributes significantly to the noise and we can calculate the A-weighted input referred noise caused by the thermal noise of R_{out} as

$$V^2_{ninR_{out},rms} = \frac{4kT}{R_{out} g_m^2} \left(\frac{C_m + C_p + C_g}{C_m}\right)^2 \cdot 12448.6 \tag{166}$$

coefficient 12448.6 is calculated in the chapter about noise optimization and is due to A-weighting of thermal noise in the 20Hz-20kHz band. Again, plugging in for optimal transistor noise $\frac{C_m+C_p+C_g}{C_m} = 2.2$ and plugging in g_m for I_D=$50\mu A$ and $ifor = 2$ it can be calculated that $V_{ninR_{out},rms}$ is less than $0.1414\mu V_{rms}$ (10% transistor noise) for R_{out} larger than $8.43k\Omega$. Previously calculated value of $7k\Omega$ for having gain 2.5 is acceptably close to this value.

For an amplifier with gain 2.5, the amplitude of a single-ended output signal when using two microphones for maximum sound pressure level (20Pa) is 300mV. For a resistor value $7k\Omega$ and $50\mu A$

$M_{1,2}$	600/3	$\mu m/\mu m$
$R_{1,2}$	8.9	$k\Omega$
M_3	120/1	$\mu m/\mu m$
M_4	60/1	$\mu m/\mu m$
D_{1-6}	0.45, 0.45	$\mu m, \mu m$
D_{p1-p4}	1, 1	$\mu m, \mu m$
C_c	30	pF
C_f	12	pF
C_{5-6}	1	pF

Table 7: Component dimensions of the preamplifier from Fig. 49.

through a transistor, the output common-mode voltage is 350mV which is acceptable. For this output common-mode voltage, not to limit the output voltage swing, the voltage on the output transistor drain $V_{out+,out-}$, should be larger than 650mV. Further more, to allow operation of the input transistors (M_1 and M_2) and the current source M_3 in saturation, the condition $V_{out+,out-} < V_{DD} - V_{DSat1,2} - V_{DSat3}$ should be fulfilled. As the minimum operating voltage V_{DD} is 1.6V (for telecom applications), the maximum voltage at the sources of M_1 and M_2 should be around 1.3V and the maximum M_1 and M_2 drain-source saturation voltage $V_{DSat1,2}$ 1.3V-0.65V=0.65V.

An important property of the amplifier is its total harmonic distortion (THD). It is explained in [7] that the THD of a common-source as well as a differential pair is minimal for input transistors working in moderate inversion, thus our choice of $ifor$ close to 2, is in line with this requirement. It is known [4] that a common-source stage has much larger distortion than a differential stage, in both cases distortion can be improved by source degeneration. Normally, voltage drop on the source resistor decreases voltage headroom and the source resistor increases noise, and it is not investigated in details if using a source degenerated differential pair would be beneficial for our application here.

In this implementation voltages at the gates of input transistors vary as a function of time. Because the transistor current generated by the current mirror M_3 determines the gate-source voltages of $M_{1,2}$, their source voltages will follow changes of the gate voltages ($V_{S1,2} = V_{GS1,2} + V_{G1,2}$). Further more, the voltage at the transistor gate has to be lower than the supply voltage minus gate-source voltage of M_1 minus M_3 saturation voltage at any time i.e. $V_{G1,2}(t) < V_{DD} - V_{GS1,2} - V_{DSat3}$. The final value of $V_{G1,2}$ is determined by the output common-mode voltage of the feedback amplifier FA (Fig. 49), set by its common-mode feedback circuit, plus the voltage over the back-to-back diodes $D_{1,2}$ and $D_{3,4}$. Voltage over the back-to-back diodes $D_{1,2}$ and $D_{3,4}$ changes as a function of time as well and for having a non-significant noise contribution (chapter on noise optimization) the resistance they present should be tens of $G\Omega$ at any time. This is achieved for a voltage over diodes less than 300mV, as it will be seen. The output common-mode voltage set by the FA CMFB circuit is 0.6V.

The design tradeoffs and calculations described here have been confirmed by BSIM3v3 simulations, giving very close results. The final transistor dimensions chosen, based on simulations, are W=600μm

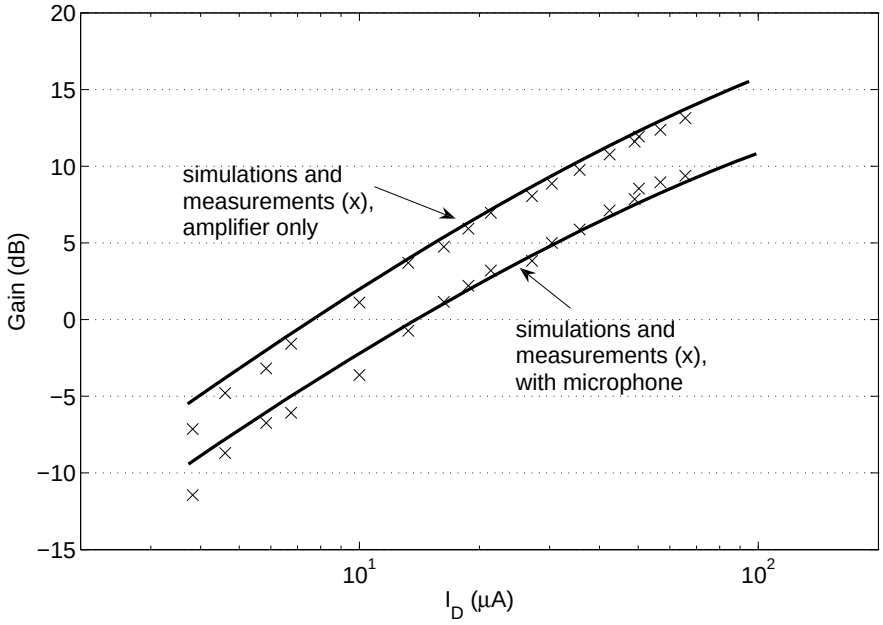


Figure 50: Simulated and measured amplifier gain vs. bias current (W=600μm and L=3μm).

and L=3μm which is less width than the calculated optimum, and the load resistor chosen was $R_{1,2} = 8.9k\Omega$ giving gain 2.5 at 53μA and $ifor = 3.2$. Components of the circuit from Fig. 49 are shown in Table 7.

9.2.3 Design Methodology Verification

To verify the design methodology used measurement results on the designed amplifier are compared with BSIM simulations and calculations in the figures to follow. In Fig. 50 simulated and measured differential gain versus transistor drain current is compared with measurement results on the amplifier from Fig. 49 with input transistor dimensions W=600μm and L=3μm when the measurements are done on the amplifier only (C_m connections short-cut) and when the gain obtained from acoustical measurements is divided by the microphone sensitivity of $4.2\frac{mV_{rms}}{Pa}$ (10V microphone bias voltage). It can be noticed that the simulations match well measurement results.

To verify the noise calculations using EKV model, where default $\eta = 1.3$ is used as well as μ from a transistor parameter file, in Fig. 51, transistor g_m is compared with simulations and in Fig. 52 flicker noise calculations are compared with measurement results in both cases as a function of transistor drain current and for W=600μm and L=3μm. The results shown, approve well the usage of the EKV model in calculations.

The factor $\left(\frac{C_m+C_p+C_g}{C_m}\right)$ is plotted in Fig. 53 when calculated using EKV model with $C_m = 5.6pF$ and $C_p = 0.5pF$, it is plotted when gain simulations results of the circuit from Fig. 49 with the microphone model are divided by gain simulation results with the microphone inputs short-cut, and thirdly when extracting the gate-source and drain-source capacitance from simulations and using $C_m = 5.6pF$ and $C_p = 0.5pF$ in calculations. It can be seen that the calculated value of the transistor gate

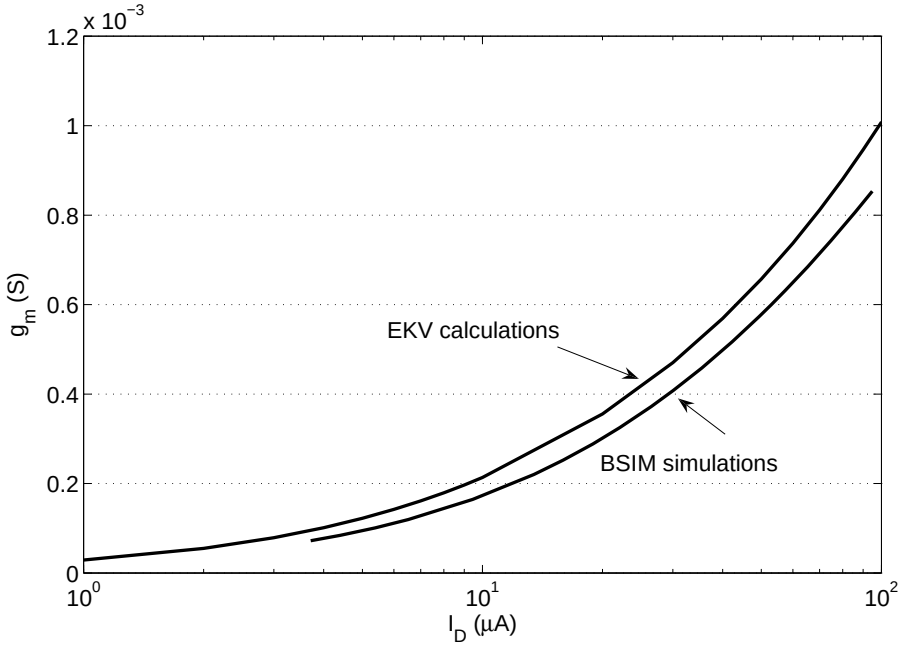


Figure 51: Simulated and calculated g_m vs. bias current (W=600μm and L=3μm).

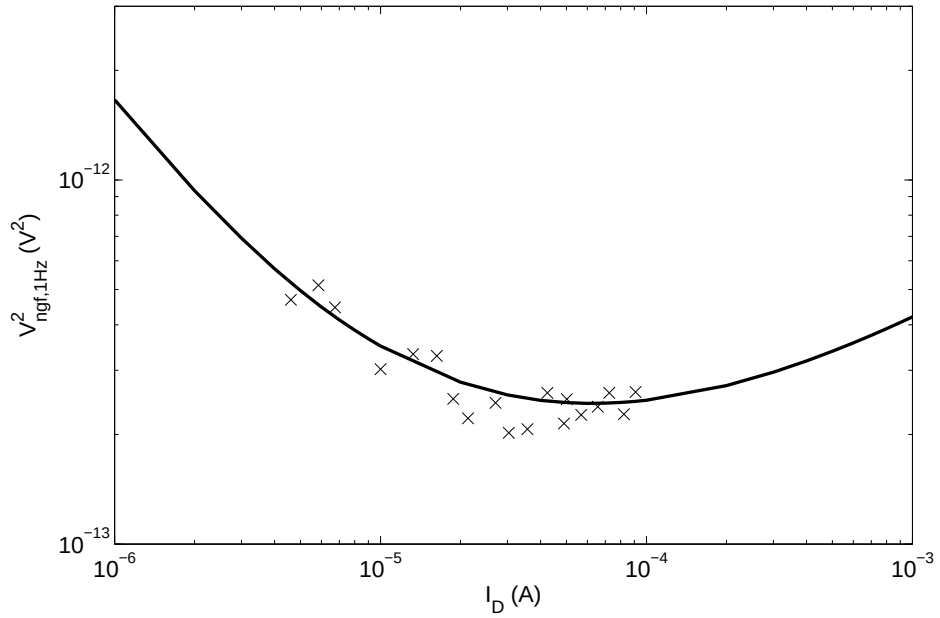


Figure 52: Measured and calculated input referred amplifier flicker noise at 1Hz vs. bias current (W=600μm and L=3μm).

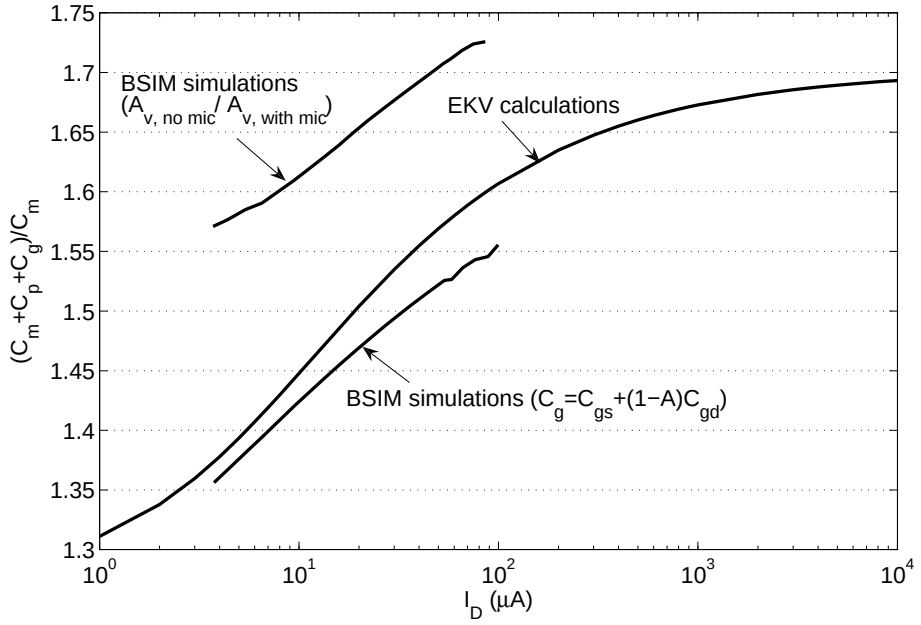


Figure 53: Simulated and calculated factor $\frac{C_m+C_p+C_g}{C_m}$ vs. bias current (W=$600\mu m$ and L=$3\mu m$).

capacitance using transistor capacitances obtained by simulations is very close to the one calculated using EKV model. Comparing the calculations for a transistor gate capacitance to the value obtained when dividing the two differential gains, the difference is around 15% and shows the influence of the coupling capacitor C_c, microphone parasitic capacitance, capacitances of the pump decoupling diodes and biasing diodes; We estimate this difference as being low enough to consider the calculations valid.

Finally, in Fig. 54, the amplifier A-weighted, rms, input noise is shown as a function of transistor drain current. SNR calculated as a function of the transistor drain current with the microphone noise $2.48\mu V_{rms}$ is shown on the same figure. As expected, increasing the bias current, does not increase SNR (decrease noise) significantly.

For the sake of completeness we mention that it can be calculated that using transistors as active load for the purpose described (two microphones differential preamplifier) it would be difficult to achieve the required low noise value, the gain would be high causing clipping of the signal for a maximum sound pressure, an output common-mode feedback would be needed due to use of active devices and it would not be possible to control the gate voltages of the input transistor as done here as the current control of the input transistors gate voltages is based on having a stable output common-mode voltage provided by current from M_3 equally divided between the input transistors.

9.3 Feedback Amplifier (FA) - Equalizing the Voltages at the Input Transistor Gates

In some implementations of a microphone preamplifier for one microphone, high impedance bias elements (back-to-back diodes) are connected between the input transistor gate and ground. This means that the transistor gate voltage is zero (or close to) at steady-state. To provide a non-zero DC bias a

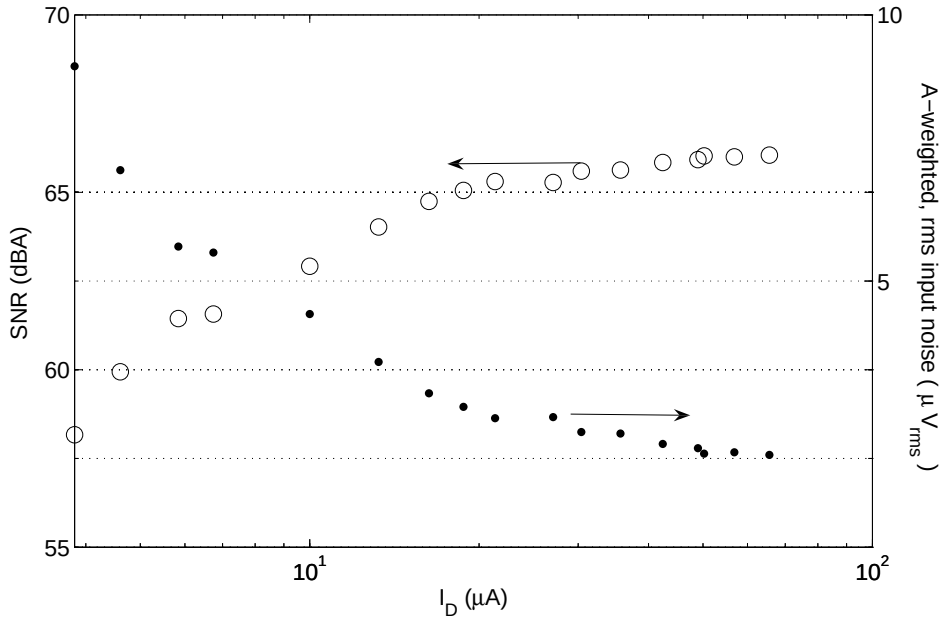


Figure 54: SNR and A-weighted input referred noise vs. bias current (W=600μm and L=3μm).

feedback amplifier can be used [6], [8].

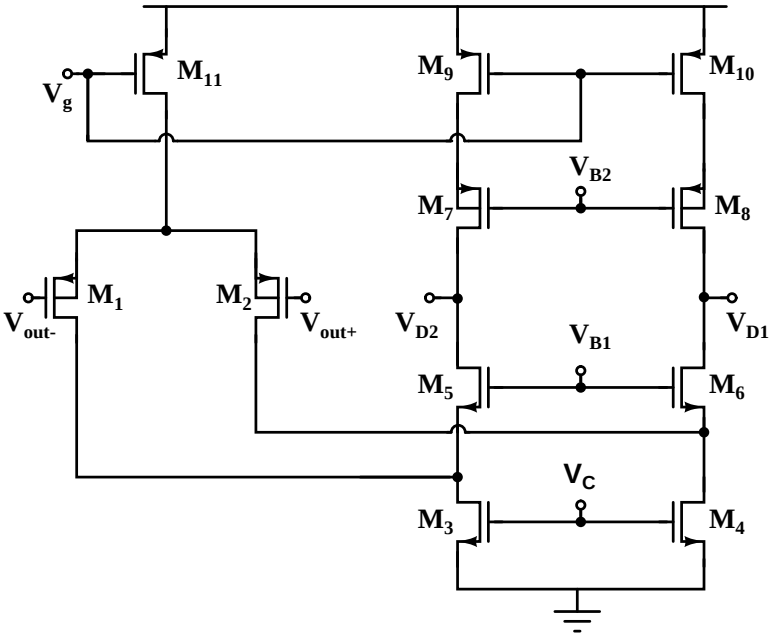
The feedback amplifier FA shown in Fig. 49, provides a non-zero DC bias at the gates of M_1 and M_2 and speeds up the start-up transient. If no FA is used, the different polarities of bias voltages V_b and $-V_b$ would unbalance the voltages at the gates of M_1 and M_2 during start-up, causing entire bias current from M_3 to flow through M_2; M_1 gate voltage starts falling from about one diode voltage while the M_2 gate voltage is close to zero Volts.

Because of the back-to-back diodes, the circuit time constants are very high and simulations show that first after hundreds of seconds the two gate voltages would be equal and the proper functionality established. The FA forces the two gate voltages to be equal after much shorter time, resulting in settling time for a full-scale differential gain of below 3s.

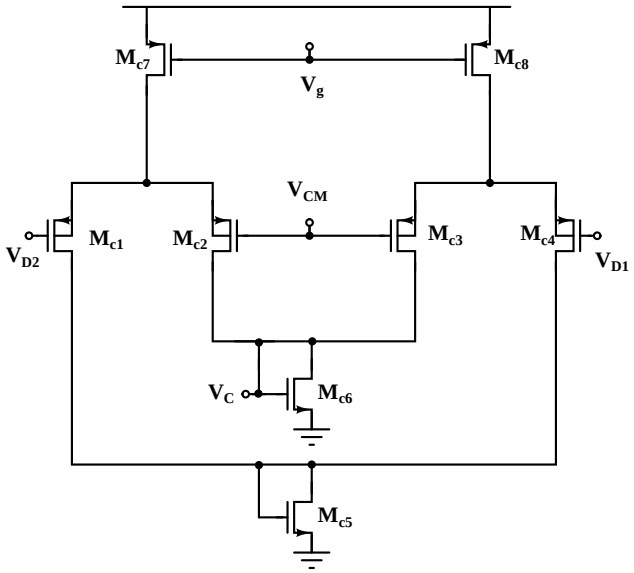
The final value at the input transistor gates, when the voltage across the diodes $D_1 - D_4$ is zero, is equal to the value set by the common-mode feedback circuit of the FA. Until that final transient value is reached, voltages on the gates of M_1 and M_2 vary and the currents through the diodes $D_1 - D_4$ diminish. Gate-source voltage of M_1 and M_2 is determined by the current provided by M_3 (which is equally divided due to the FA) and the drain voltage of M_3 follows the changes on the $M_{1,2}$ gates. Clearly, a care should be taken in the design that M_3 drain voltage is always low enough so that it operates in saturation.

A good property od this topology is that no matter how low-leakage the biasing diodes are, or how slowly the voltages at the transistor gates drift, as long as the two gate voltages are equal, which is controlled by the FA, the preamplifier is functional. This is different for a single transistor amplifier, in which case any change at the input transistor gate influences the voltage at the output.

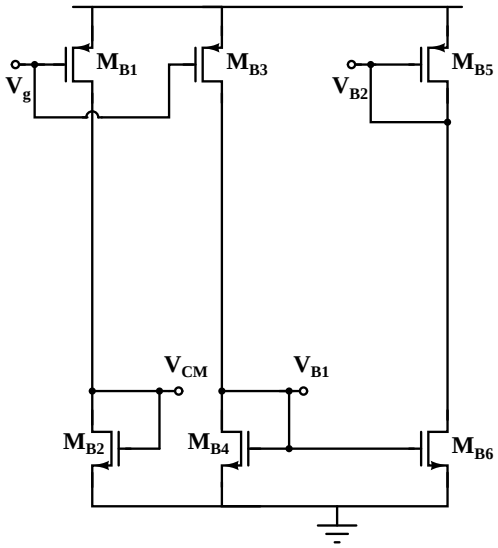
To be able to equalize the two gate voltages, the gain of the FA should be high. Due to this high



(a) Feedback amplifier FA



(b) Feedback amplifier FA common mode feedback



(c) Bias circuit

Figure 55: Top: Feedback amplifier FA. Bottom left: Common-mode feedback circuit for the FA. Bottom right: Bias circuit used.

gain, a part of the amplifier output signal fed back by the FA and appearing at its output is high, and it interferes with the normal operation of the main amplifier causing a severe distortion. A method to suppress this deleterious behavior used here was to limit the feedback signal by the diodes at the output of FA; for the purpose of the latter, diodes D_5 and D_6 are used. Capacitors C_5 and C_6 are used to ensure the stability of the FA. The feedback amplifier FA is implemented as a standard folded cascode design with a standard common mode feedback as shown in Fig. 55.

9.3.1 Fully Differential Folded Cascode Amplifier

The feedback amplifier from Fig. 49 is shown in Fig. 55 with its common-mode feedback circuit (CMFB). Input of the feedback amplifier is connected to the output of the main amplifier and the feedback amplifier input common-mode voltage is 0.47V in normal operation. Therefore a pMOS input pair is chosen. Common-mode input voltage range is

$$-V_{GS1,2} + V_{DSat1,2} + V_{DSat3,4} < V_{in,cm} < V_{DD} - V_{GS1,2} - V_{DSat11} \tag{167}$$

The feedback amplifier output common-mode voltage sets the final value on the gates of the input transistors of the main amplifier and it is chosen to design it with $V_{out,cm}$ equal 0.6V. The output voltage swing of the folded-cascode amplifier is

$$V_{DSat3,4} + V_{DSat5,6} < V_{out} < V_{DD} - V_{GS1,2} - V_{DSat11} - V_{DSat5,6} \tag{168}$$

Gain of the folded-cascode amplifier is given by $g_{m1,2}R_{out}$, $R_{out} = \frac{1}{2}g_m r_{ds}^2$ is the output resistance and the frequency of the dominant pole is $\frac{1}{2\pi R_L C_L}$ where R_L and C_L are load resistor and capacitor respectively. Unity gain frequency is $\frac{g_m}{2\pi C_L}$. The design of a folded-cascode amplifier is described in any textbook [9], [10]. Simulated gain of the FA amplifier designed is 80dB, dominant-pole $134Hz$ and unity gain frequency 1.6MHz with 1pF load. The input referred noise of a folded-cascode amplifier is,

$$V_{nin} = 2V_{n1,2}^2 + 2\left(\frac{g_{m3,4}}{g_{m1,2}}\right)^2 V_{n3,4}^2 + 2\left(\frac{g_{m9,10}}{g_{m1,2}}\right)^2 V_{n9,10}^2 \tag{169}$$

however its noise contribution is not critical in our application.

To equalize the two input voltages of the main amplifier the feedback amplifier gain should be 40dB minimum, and the settling time is less with a higher gain amplifier. However, another type of a differential amplifier which is able to sink and source small amounts of output currents might be possible to use as well such as a fully symmetrical differential OTA.

The simplest solution of a common-mode feedback circuit is used here, a standard co called long-tail pairs CMFB [10]. P-channel transistors are used as the input pairs of the CMFB circuit, as the output common-mode voltage of the folded cascode should be 0.6V what is lower than V_{GS} plus V_{DS} needed in case an nMOS input was used. Gain of the CMFB loop can be calculated as

$$A_{vCMFB} = k g_{mc1,2,3,4} R_{out}, \quad k = \frac{I_{M3}}{I_{MC6}} \tag{170}$$

where I_{M3} is the current of M_3 and I_{MC6} is the current of M_{C6}. A detailed analysis of the fully-differential folded-cascode amplifier with its CMFB circuit can be found in [11] where all the design

parameters are summarized, frequency analysis of the amplifier and the CMFB presented, stability conditions given and a procedural design scenario explained.

The feedback amplifier uses $6\mu A$ from 1.8V supply with CMFB and bias circuit. It can be investigated as future work if another type of CMFB and or differential amplifier used as a feedback amplifier in our amplifier for two microphones would give some improvements.

9.4 Practical Implementation

The amplifier is implemented in a $0.18\mu m$ 3M triple-gate triple-well CMOS process. The size of the CMOS chip is 3.2mm×0.93mm. Photo of the amplifier is shown in Fig. 56 top. This chip size is larger than necessary and is chosen to fit a package of an existing product without redesign.

A chip-scale package (CSP) of a commercially available digital microphone with dimensions $2.6 \times 1.6 \times 0.865 mm^3$ is shown in Fig. 57 [12]. The CMOS chip and the MEMS microphone chip are flip-chip mounted onto a silicon substrate. Contacts between the microphone and the amplifier are provided with negligible parasitic capacitances through connections on the substrate. A pair of substrate dies for a single microphone CSP shown in Fig. 57 is used for assembling the two microphone dies and the preamplifier for the two microphones.

The CMOS chip shown in Fig. 56 top is mounted across the two substrate dies and the existing connections on the substrates are used for connections with the two microphones. In Fig. 56 to the left, bottom view of the two substrate dies is shown, the top view of the microphones and the amplifier mounted is shown to the right and in the middle is the test PCB with the mounted component. A microphone membrane radius is 1.05mm and the size of the CSP for two microphones and the amplifier is $2.6 \times 3.2 \times 0.865 mm^3$.

Concerning the amplifier layout, for a minimal threshold voltage mismatch the input transistor pairs are connected in a cross-coupled configuration using unity size transistors (also for folded-cascode input pairs and CMFB circuit input pairs). Dummy structures are used wherever needed. $A_{V_{th}}$ for cross-coupled 6V pMOS transistors is $6.8778 \text{mV}\mu m$, and for 6V nMOS $12.0115 \text{mV}\mu m$. High ohmic resistors are used for the two drain resistors loading the input pair and are implemented using unity size resistors connected in a serpentine where each of the units is surrounded either by a dummy resistor or units of the other matching resistor. Capacitors are implemented using unity size capacitors as well. Deep n-wells are connected with care at their proper potential to avoid unwanted leakage.

9.5 Measurement Results

Measurement results on the CSP will be presented in this subsection. The nominal transistor bias current chosen for the design is $53\mu A$. Acoustical measurements are done using anechoic pyramid testbox TBS50 by Interacoustics with frequency range 60Hz-9kHz. For results previously presented in the chapter describing design tradeoffs a smaller test box by the same manufacturer was used and therefore a minor difference in the results might be observed. The results from the larger pyramid are exact.

Measured differential output voltage for a sound pressure level, SPL, of 94dB (i.e., 1 Pa) and

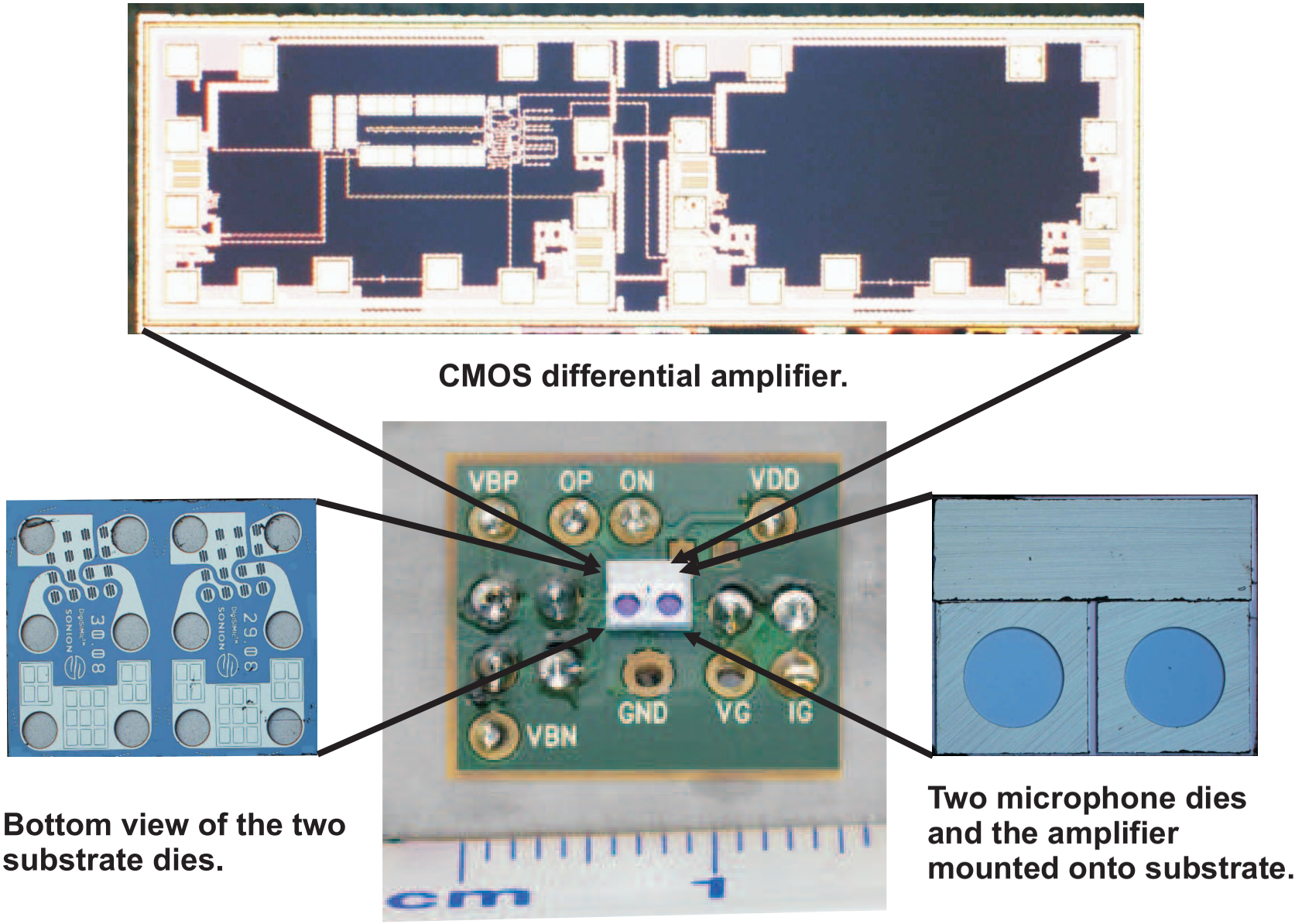


Figure 56: Top: Preamplifier chip photo. Center: Measurement PCB with the CSP. Left: CSP bottom view. Right: CSP top view.

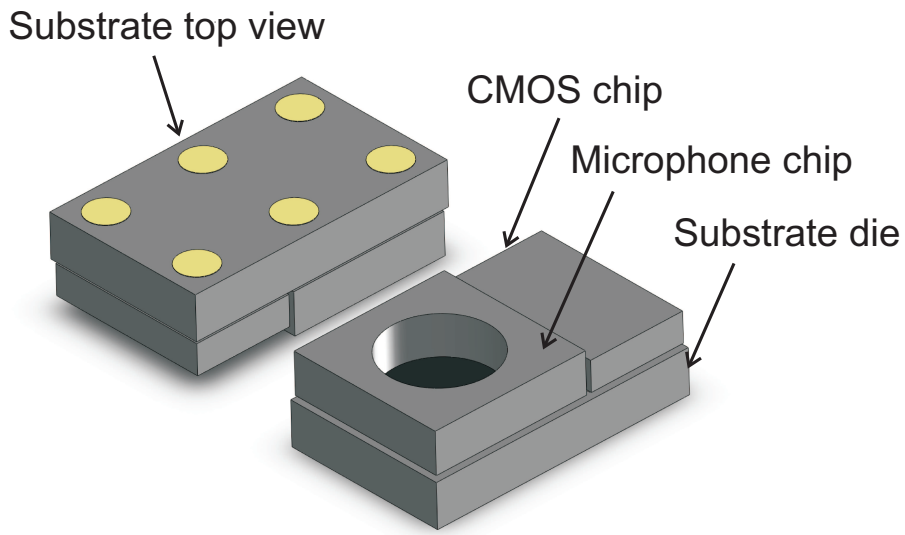


Figure 57: Pulse's commercially available digital microphone CSP - a pair of its substrate dies is used in this work without redesign.

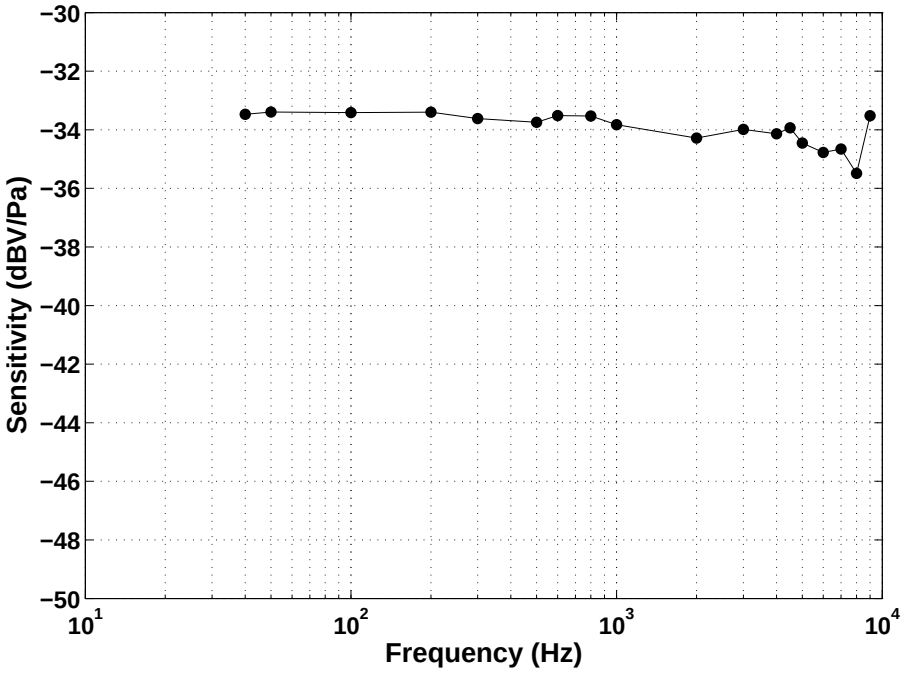


Figure 58: Frequency response of the CSP.

V_b=±10V at 1kHz is 21mV_{rms}; with an amplifier gain of 8dB, the resulting sensitivity of the two-microphones only is 8.4mV_{rms}/Pa. Frequency response under the same conditions was measured for the frequency range allowed by the testbox used, and is shown in Fig. 58. The sensitivity is -33.5dBV_{rms}/Pa and the transfer function is expected to be flat until at least 20kHz.

A plot of the THD as a function of the sound pressure level at 1kHz is shown in Fig. 59. No

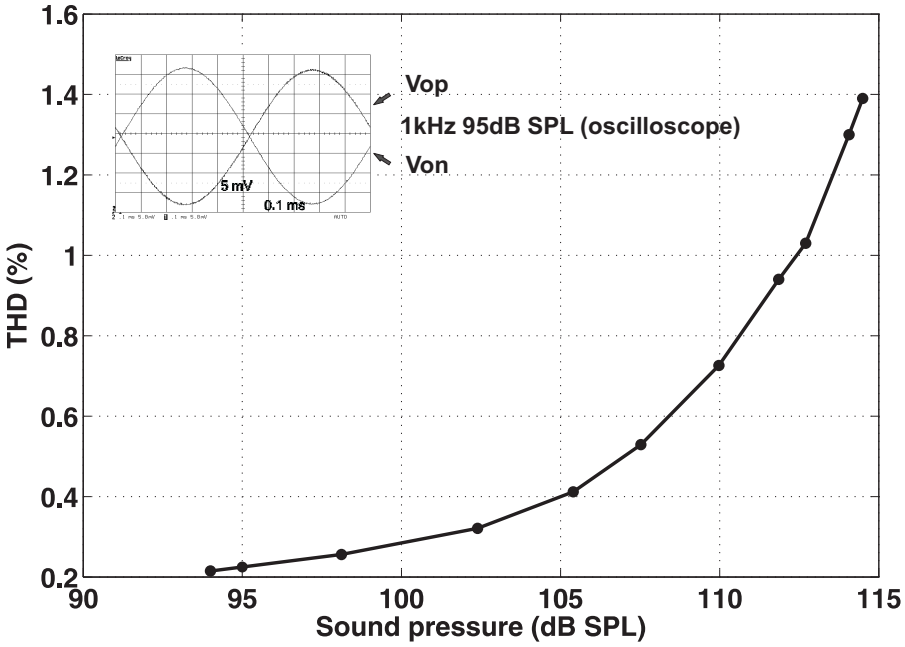


Figure 59: THD of the output signal vs. sound pressure level.

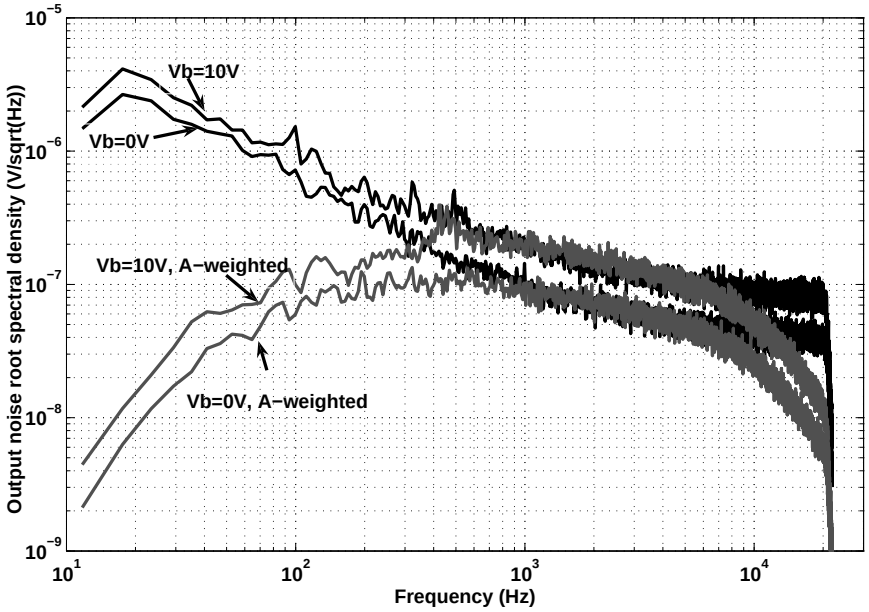


Figure 60: Differential output noise of the CSP with and without microphone bias and with and without A-weighting filter.

significant distortion due to the feedback amplifier can be noticed, and the THD is below 1% for an SPL below 112dB. Amplifier output voltages V_{out+} and V_{out-} or (V_{op} and V_{on}) for an input 1kHz 95dB SPL are shown as an inset in the latter figure.

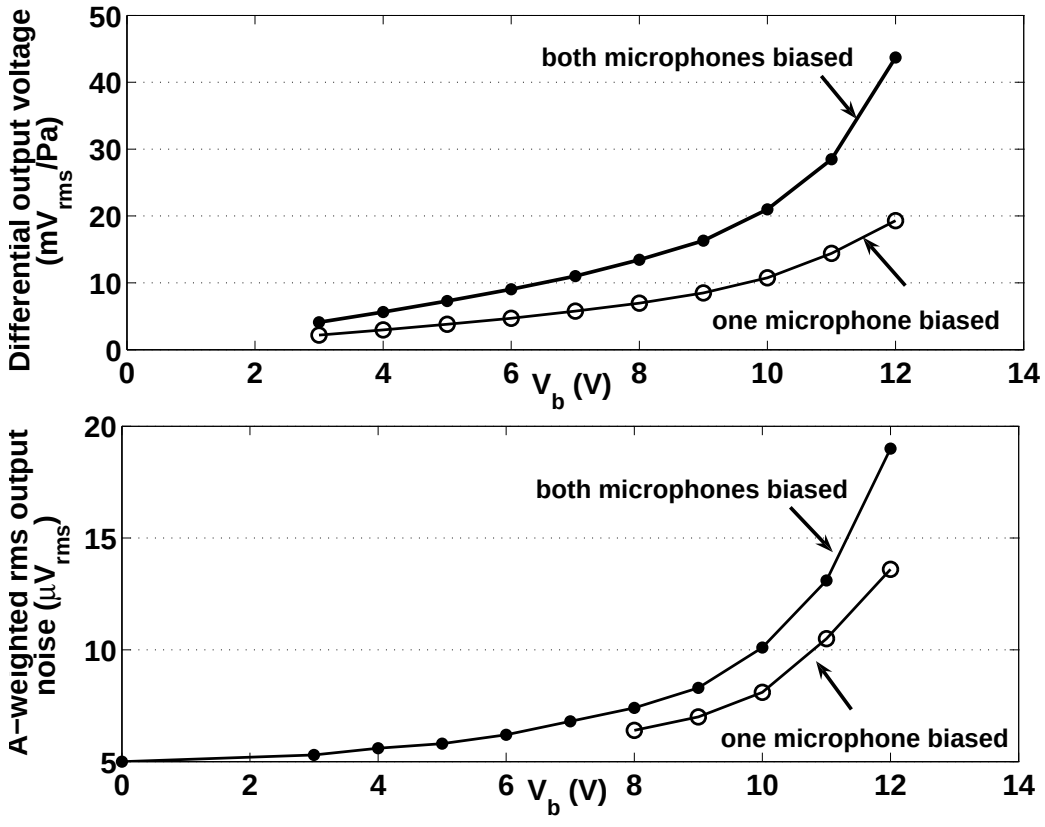


Figure 61: Top: Differential output voltage vs. microphone bias. Bottom: A-weighted differential output noise vs. microphone bias.

In Fig. 60 a plot of the differential output noise spectral density is shown when the microphone bias is zero volt, i.e. only amplifier noise is measured and when the bias on the two microphones is 10V, i.e. the sum of the noise contribution of the two microphones for 10V bias is measured together with the amplifier noise. It can be seen that the flicker noise corner is around 4kHz. The influence of the A-weighting filter which is used as a standard for acoustical measurements because it follows the sensitivity of a human ear is shown in the same figure when $V_b = 0$ and when $V_b = 10V$. It can be calculated that the measured flicker noise has slightly higher impact compared to the white noise, when both contributions are A-weighted. The expected SNR degradation introduced by the amplifier is lower than 1.5dB for Vb=+-10V.

As shown in Fig. 61 (top) increasing the microphone bias voltages increases microphone sensitivity, resulting in higher microphone output voltages. However, if V_b reaches 12.2V, the microphone collapses, with the membrane sticking to the bottom plate. Functionality can be restored by discharging the microphone to 0V. The A-weighted 20Hz-20kHz rms differential output noise is also shown in Fig. 61 (bottom). At low V_b values, noise is almost totally coming from the amplifier ($5\mu V_{rms}$), while at higher V_b values the microphone noise becomes dominant. In the same figure (Fig. 61), output voltage and output noise are shown versus microphone bias if only one microphone is biased.

The SNR vs. V_b is shown in Fig. 62, where a very good SNR of 66.5dB is achieved at V_b=10V

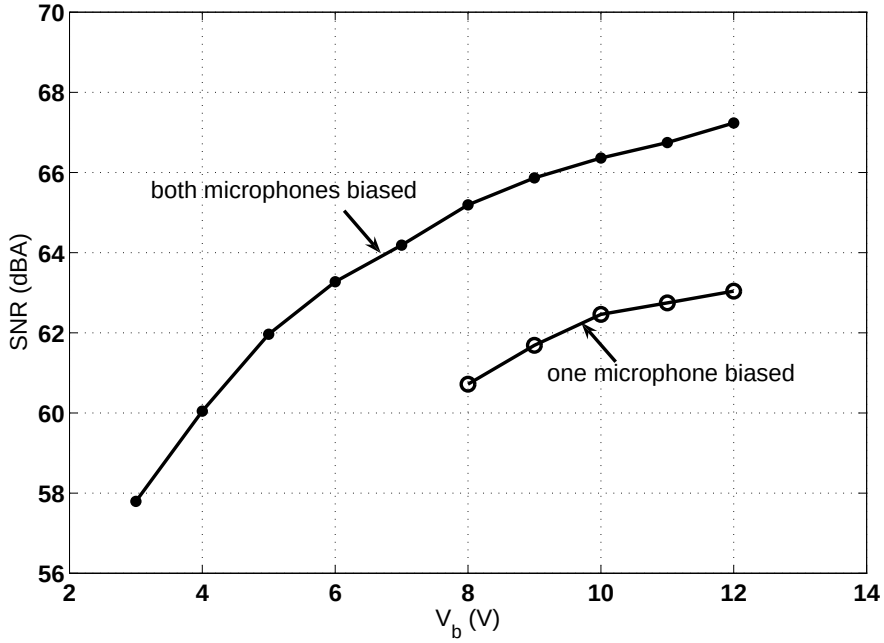


Figure 62: SNR vs. microphone bias when both microphones are biased and when one microphone is biased.

(the SNR drops by only 1dB at a more conservative V_b of 8.5V). For the nominal condition V_b=10V, the SNR deterioration caused by the amplifier is ∼1.0dB. The same figure shows that using only one microphone reduces the SNR by some 3-4dB, as expected. The amplifier consumes $120\mu A$ at 1.8V supply.

Table 8 presents a comparison with other MEMS microphone products with data from available data sheets. It can be seen that our work has several dB higher SNR. Due to Pulse's compact packaging, the new microphone CSP occupies a very small area despite the use of two microphone dies. Its area is smaller than the area of products having a standard 4.7mm×3.7mm footprint and using only one die. Smaller are only Pulse's own analog microphone [13] using one MEMS die and [14] which has been announced very recently. Other good properties of this work are a flat frequency response, good PSRR, low THD. It can be seen that the state-of the art MEMS microphones with a single microphone have maximum SNR around 62dB which is too low for requirements for applications such as hearing instruments. Our solution with 3dB SNR increase makes MEMS microphones much closer to fulfilling specifications for this new potential application.

9.6 High Resistance On-Chip Implementation

In the design of a microphone amplifier high resistor values are needed. A high resistances is needed to isolate the charge pump providing the microphone bias voltage and the microphone (Fig. 48, 49). The resistance that provides a DC path from the gates of the input transistors that amplify the microphone signal to ground, shown in (Fig. 49) has to be extremely high as well to place the lower cut-off frequency

	Size, smallest available (mm)	**Sensitivity (dBV @1Pa, 1kHz)**	**SNR (dB@1Pa, A-weighted)**	**Response (Hz)**	**V_{sup} (range) (V)**	**I_{sup} (μA)**	**PSRR (dB)**	**THD (%@dB SPL, 1kHz)**	**R_{out} (Ω)**
this work	**2.6×3.2×0.865**	**-33**	**65.5**	**20-20k**	**1.8 (1.6-3.6)**	**120**	**>55**	**0.4@104**	**8.9**
[13]	2.33×1.6×0.865	-40	61	20-20k	1.8 (1.64-2.86)	330	>60	2@104	500
[14]	2×2×1.25	-33 to -45	57		(1.65-3.6)	140	>45	5@115	
[15]	4.72×3.76×1.25	-42	59	100-7k	2.1 (1.5-3.3)	80	55	0.1@104	7
[16]	4.72×3.76×1.25	-22 or -42	59	100-10k	(1.5-3.6)	<350 or <250	>40	1@100	<300
[17]	4.72×3.76×1.25	-35 to -30 or -40 to -35 or -45 to -40	57	100-7k	2.1 (1.5-3.6)	120	45	1@104	100
[18]	4.72×3.76×1	-37	62	100-12k	1.8 (1.5-3.6)	200	>50	3@105	200
[19]	4.72×3.76×1.25	-42	57	100-16k	(1.5-3.6)	150			100
[20]	4.3×3.4×1.28	-42	55		(1.5-3.6)				
[21]	3×4×1	-44	55		2	500			

Table 8: Performance comparison with commercially available products.

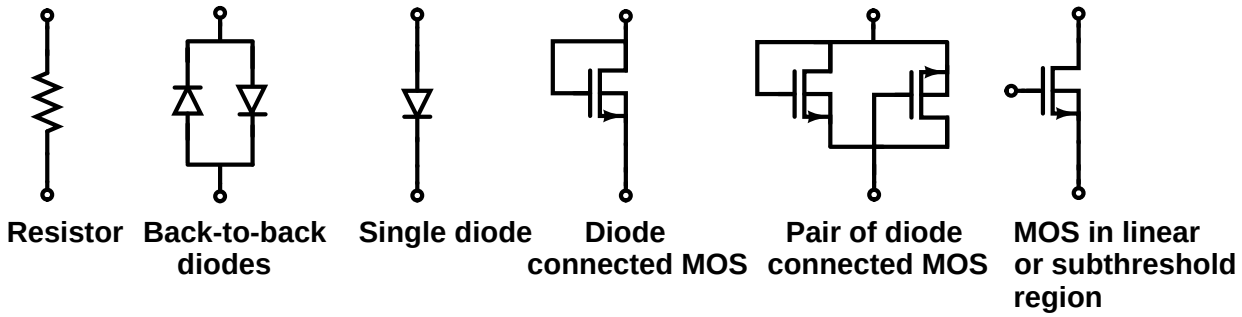


Figure 63: Possible high resistor implementations.

of the amplifier transfer function well below 20Hz. As explained in the chapter on noise optimization an additional reason for the biasing resistance being large is to minimize its noise contribution.

High resistances on-chip can be implemented in several ways, shown in Fig. 63. A simple solution of a resistor implementation is a MOS transistor working in the linear region with its resistance given by

$$R_{DS} = \frac{L}{W}\frac{1}{\mu C_{ox}(V_{GS} - V_T)} \tag{171}$$

where R_{ds} is the drain-source resistance.

Methods of implementing high resistances on-chip are explained in works dealing with bioamplifier designs such as [22]-[24]. In [24] a usage of a MOS-bipolar pseudoresitor element (a diode-connected pMOS transistor with the bulk n-well connected to source) is described. For negative gate-source voltages in that design, the diode connected pMOS transistor is activated and for positive gate-source voltages, the parasitic p-n-p (source-well-drain) bipolar transistor is activated working as a diode connected bipolar junction transistor. Some other works [23] use transistors biased in the subthreshold region for implementing similar high resistances as the conductance of a MOS transistor in the subthreshold region can be expressed by

$$\frac{dI_{DS}}{dV_{DS}} = \frac{1}{R_{DS}} = \frac{I_{D0}}{V_{th}} exp\left(\frac{V_{GS} - V_T - V_{off}}{\eta V_{th}}\right) exp\left(\frac{-V_{DS}}{V_{th}}\right) \tag{172}$$

with $I_{D0} = \mu V_{th}^2 \frac{W}{L} C_{ox}$. V_{off} is defined as the offset voltage determining the channel current at V_{GS}=0. Unless the transistor working in the subthreshold is diode connected ($V_{GS} = V_{DS}$), this solution of implementing high resistances requires an additional bias voltage for providing the transistor gate voltage.

Other high resistor implementation proposals exist as well, in [25] a high resistor is implemented using a switched capacitor circuit and in [26] using an operational transconductance amplifier (OTA). Traditionally for biasing a microphone preamplifier input transistor back-to-back connected diodes or diode connected transistors have been used. A resistance presented by a diode can be expressed by

$$\frac{dI_D}{dV_D} = \frac{1}{R_D} = I_S\left(e^{V_D/\eta V_{th}} - 1\right)\frac{1}{\eta V_{th}} = \frac{I_D}{\eta V_{th}} \tag{173}$$

where I_S is a diode saturation current proportional to diode area, V_D diode voltage, η diode characteristic slope factor and V_{th} thermal voltage.

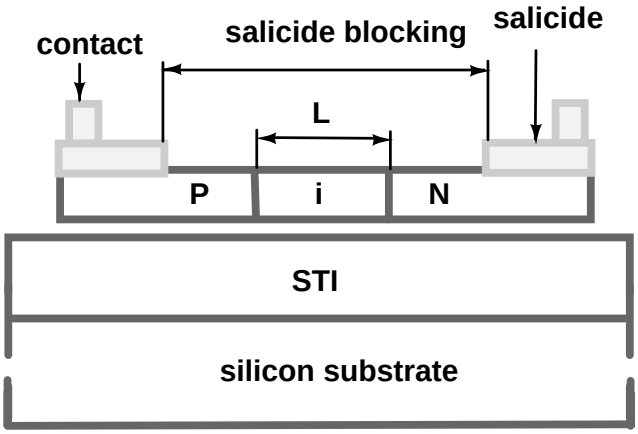


Figure 64: Polysilicon diode cross section.

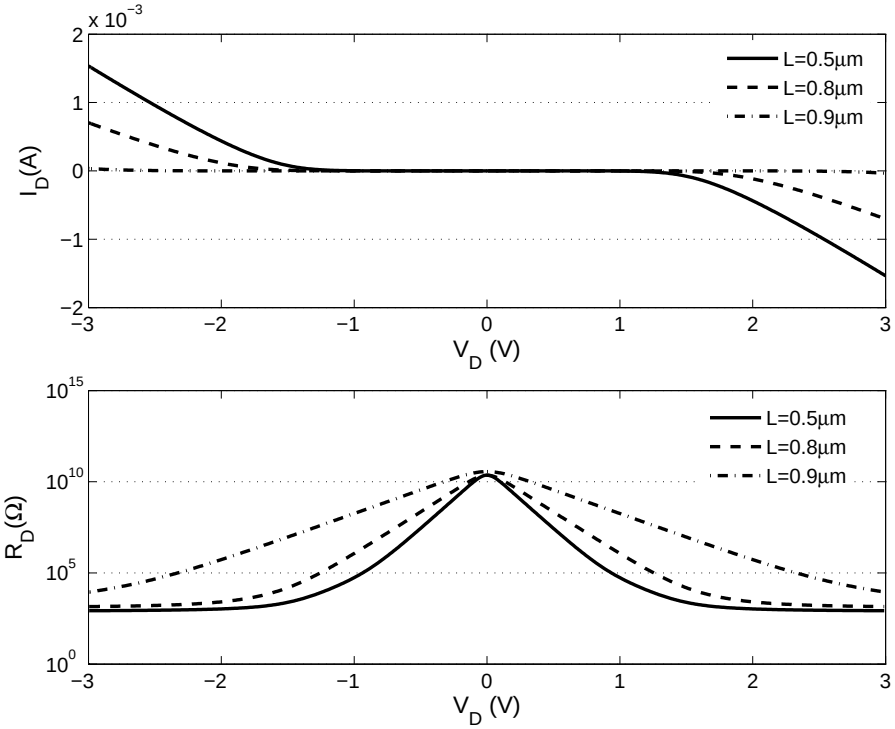


Figure 65: Top: Back-to-back polysilicon diodes I-V characteristics. Bottom: Resistance presented by the back-to-back polysilicon diodes.

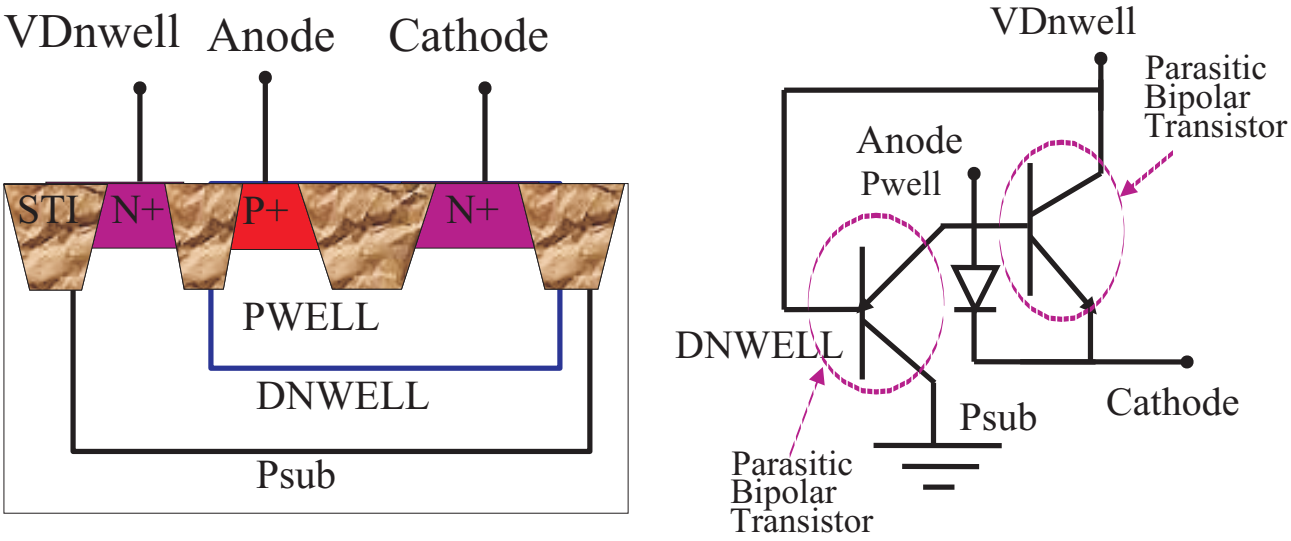


Figure 66: N^+p-well diode inside a deep n-well.

In this work, one of the microphones is biased with a voltage of negative polarity and to avoid latch-up and leakage, it is chosen to use polysilicon diodes for high resistance isolation of the microphone and the charge pumps shown in Fig. 48.

A cross-section of the polysilicon diode is shown in Fig. 64. A polysilicon diode has p-type and n-type highly doped regions in a polysilicon layer. The length of the un-doped polysilicon region between n^+ and p^+ regions, L, influences the diode $I-V$ characteristics. The whole diode polysilicon layer is deposited over a gate oxide layer and under the gate oxide layer is a shallow-trench-isolation layer under which the silicon substrate is placed. Manufacturing is done that an intrinsic polysilicon layer is deposited after the gate oxide growing, followed by the doping of the highly doped regions with the same process steps as used for MOS source/drain implantation [27]. The polysilicon diode has no p-n junction in the common substrate, allowing isolation of positive and negative voltages from the substrate.

In Fig. 65 top, a simulated current-voltage $(I-V)$ characteristics of a pair of back-to-back polysilicon diodes with width $1\mu m$ and several diode lengths is shown. In the bottom of the same figure, simulation results of the resistance $(\frac{dV_D}{dI_D})$ presented by the back-to-back polysilicon diodes is shown for diodes with same lengths. The equivalent resistance presented by the diodes increases for diodes with larger length of the undoped region L. Minimum size diode available has center region L=$0.5\mu m$ and according to the simulations shown, a pair of these diodes used in a back-to-back configuration present some ten GΩ at zero current. Measurement results on the polysilicon diodes used here, are available as internal data and will not be discussed due to confidentiality issues.

To minimize the influence of the resistor used for biasing the input transistor on the noise performance of the amplifier, the resistance value of the biasing resistor should be as large as possible, and using the analysis from the chapter on noise minimization for capacitive sources, it should be larger than 50GΩ. Typically a tradeoffs exist between the requirement for a large bias resistor for low noise and fast amplifier settling time. One of the advantages of the differential topology used here

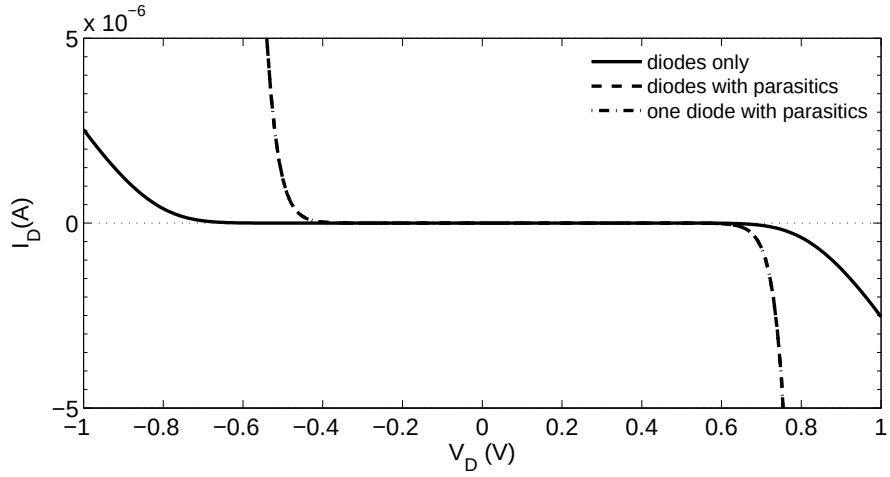


Figure 67: Back-to-back n^+p-well diodes inside a deep n-well I-V characteristics.

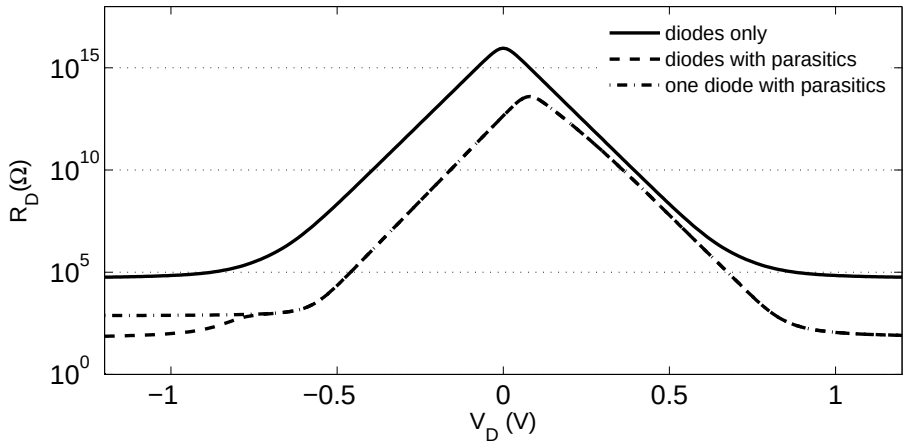


Figure 68: Resistance presented by back-to-back n^+p-well diodes inside a deep n-well.

comparing to a single transistor implementation is that the slowly varying transient voltages on the gates of input transistors due to the high bias resistor values do not pose a problem as the feedback amplifier equalizes them fast. Therefore, using back-to-back n^+-pwell junctions inside a deep n-well with an extremely high zero-current resistance ensures very low dynamic resistor noise influence at the same time not sacrificing the settling time of the amplifier.

A cross section of an n^+p-well diode inside a deep n-well is shown in Fig. 66. On the same figure a diode model is shown with the parasitic bipolar transistors between p-well, deep n-well and p-substrate and between n^+ implant, p-well and deep n-well. Simulations of the current-voltage characteristics of the two back-to-back n^+p-well diodes inside a deep n-well with the deep n-well connected to the anode are shown in Fig. 67 for a minimum size high voltage diode with W=0.45μm and L=0.45μm with and without influence of the two parasitic bipolar transistors. It is assumed that the parasitic action of the bipolar npn transistor formed between two adjacent wells and the substrate can be neglected. On the same figure simulations are also shown when using only one diode. For the latest case, for positive diode voltages the pn junction of the diode is forward biased, while for negative voltages, the parasitic junction between the deep n-well and p-substrate is active. This is similar to the method proposed in [24] where a high resistance is implemented using a MOS-bipolar element.

Simulations of the equivalent resistances presented by the back-to-back diodes, with and without parasitic elements and the single diode-bipolar element with I-V characteristics from Fig. 67 are shown in Fig. 68. For all three cases simulations show impedances larger than TΩ at zero currents. Measurement data on the diodes are available as internal data and will not be discussed. Similarly, diode connected MOS transistors can be used for implementing high resistances, again influence of the parasitic elements should be taken into consideration.

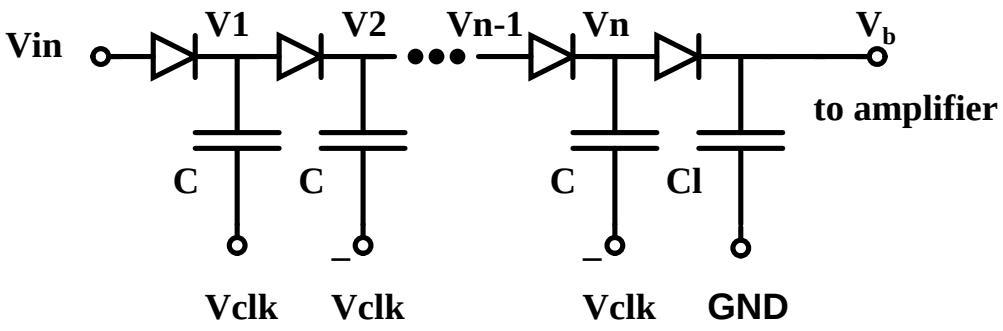


Figure 69: N-stages positive charge pump.

9.7 Charge Pump Design

Relatively high absolute values of bias voltages are needed for biasing the MEMS microphones shown in Fig. 48 and need to be generated on-chip. Charge pump circuits are used to generate on-chip voltages higher than the supply voltage and lower than ground voltage. Most often used integrated solution of a voltage multiplier (charge pump) is proposed by Dickson [28]. Voltage multipliers (charge pumps) are typically used for writing and erasing flash and EEPROM memories. In [29] a Dickson pump is used for biasing a MEMS microphone.

Dickson charge pump uses a string of diodes with nodes which are coupled through capacitors with two input clock signals in anti-phase V_{clk} and $\overline{V_{clk}}$ as shown in Fig. 69. In the analysis of this circuit, stray (parasitic) capacitances C_s need to be taken into account and are added in Fig. 70. Looking at Fig. 70, the Dickson multiplier operates by pumping charge along the diode chain as the capacitors are successively charged and discharged during each clock cycle. For a low value of the clock signal V_{clk}, the first diode conducts and the voltage V_1 at the node 1 becomes the difference between the input voltage V_{in} and the forward biased diode voltage V_D, or $V_{in} - V_D$. When the V_{clk} goes high, the voltage V_1 becomes $V_{in} - V_D + V_{clk}$. Due to this voltage, the second diode in the string will conduct and the voltage at node 2, V_2, will become $V_{in} - 2V_D + V_{clk}$. When in the next clock cycle V_{clk} becomes low again, the voltage V_2 will become $V_{in} - 2V_D + 2V_{clk}$. The diode between the N-th node and the output is used to prevent the clock breakthrough. After N stages, the output voltage V_{out} (Fig. 70) is given by $V_{out} = V_{in} + N\left(V_{clk} - V_D\right) - V_D$ [28], [30].

More accurately, the clock voltage is reduced due to the capacitive division between the stray capacitance C_s and the clock coupling capacitor C and in calculations a proportion of clock signal equal to $\left(\frac{C}{C+C_s}\right) V_{clk}$ needs to be taken into consideration. Knowing this, in the pump design, a stray capacitance should be minimized.

If some current is driven from the pump, denoted I_{out}, the final pump voltage is reduced by a value equal to $\frac{NI_{out}}{(C+C_s)f_{clk}}$ where f_{clk} is the clock frequency. This gives the final voltage at the output of the pump as

$$V_{out} = V_{in} + N\left(\frac{C}{C+C_s} \cdot V_{clk} - V_D - \frac{I_{out}}{(C+C_s)f_{clk}}\right) - V_D \tag{174}$$

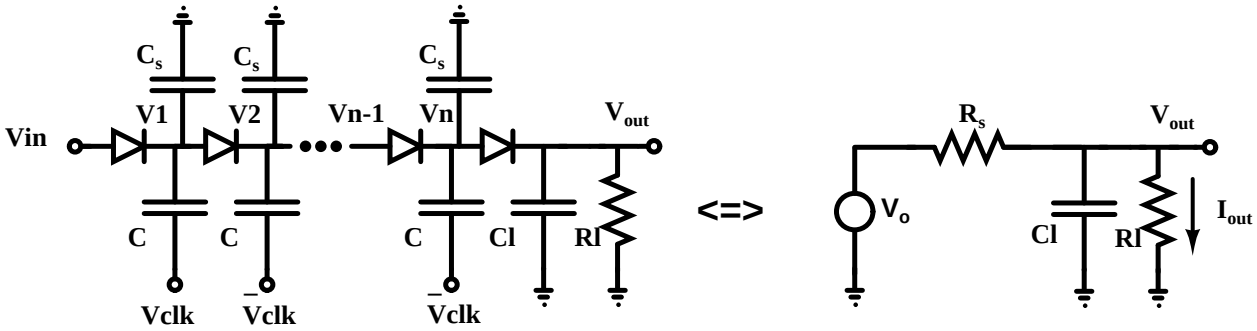


Figure 70: N-stages positive charge pump wit stray capacitances and its equivalent circuit.

It can be noticed from the latter formula, that for a multiplication to occur, $\frac{C}{C+C_s}V_{clk} - V_D - \frac{I_{out}}{(C+C_s)f}$ should be greater than zero and that condition is independent of the number of stages.

From (174) it is possible to write

$$V_{out} = V_O - I_{out}R_s \tag{175}$$

and it is possible to represent the pump with the equivalent circuit as shown in Fig. 70 on the right, where

$$V_O = V_{in} - V_D + N\left(\frac{C}{C+C_s}\cdot V_{clk} - V_D\right) \quad and \quad R_s = \frac{N}{(C+C_s)\,f_{clk}} \tag{176}$$

As further explained in [28], the ripple voltage, V_R, at the output of the pump due to the load resistance R_l shown in Fig. 70 exists and can be calculated as $V_R = \frac{I_{out}}{f_{clk}C_l} = \frac{V_{out}}{f_{clk}R_lC_l}$ where C_l is the load capacitance and I_{out} output current. Additionally an extra term equal to $\frac{C_D}{C_l}\frac{C}{C+C_s}V_{clk}$, where C_D is the capacitance of the diode, should be added in the latest formula for calculating the ripple voltage; that therm should be added if the non-overlapping clocks are used and is two times larger for overlapping clocks. As it can be seen, the ripple voltage can be reduced by increasing the clock frequency as well as using a large load capacitance. However, increasing the load capacitance, the pump reaches steady-state after longer time. In practice, the pump capacitors are not fully charged and discharged with a diode cut-off voltage V_D and there is some remaining voltage across the diodes at the end of each cycle causing the multiplier output series resistance to increase nonlinearly [28]; to minimize the increase of R_s due to this effect, a condition $R_D\,(C+C_s)\,f_{clk} < 3$ should be fulfilled.

The practical implementation of the Dickson charge pump from [28] was with a diode-connected nMOS transistors with p-substrate connected to ground. The pumping gain of the charge pump is calculated as $V_N - V_{N-1}$ which is for a diode connected transistor not driving a resistive load $\sim (V_{clk} - V_T)$, where V_T is a transistor threshold voltage. As the number of stages of the Dickson pump increases, the pumping gain is degraded due to the transistor body effect as the transistor threshold voltage decreases. Therefore, the output voltage of a MOS charge pump is lower than of a genuine diode and is not convenient for low voltage operations as the V_{clk} decreases.

Many researches have analyzed and improved the design of charge pumps. Some articles such as [31]-[34] deal with general theoretical analysis and pump modeling. In for example [35], a theoretical analysis

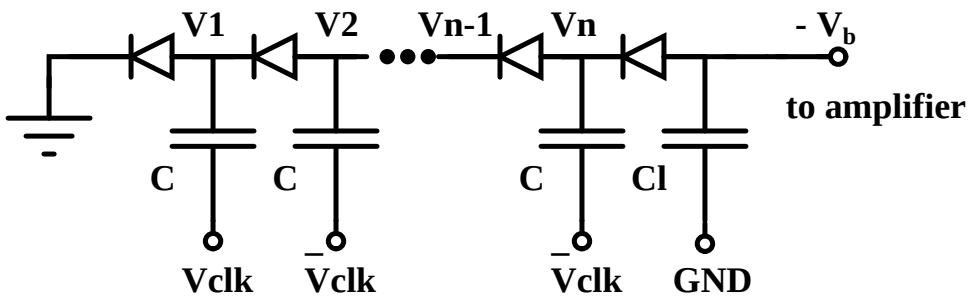


Figure 71: N-stages negative charge pump.

is applied to design optimization with capacitive loads only. Various works and pump implementations have been introduced in order to maximize a pump gain and or improve pump efficiency. To eliminate the transistor threshold voltage drop, a MOS charge pump with static charge transfer switches (CTS) is described in [36] improving a pumping gain and a low-voltage operation capabilities. Other charge pump implementations without degradation due to the transistor body effect suitable for low voltage operation are described in [37]-[39]. In [39] gate-oxide reliability issues are taken into consideration. In [40] a regulated charge pump implementation is proposed for driving large output currents.

As explained in [27], [41], even though using a pump with $p^+ - nwell$ junction diode compensates for the body effect of a MOS transistor, the charges from the cathode will leak to ground through a parasitic p-n junction existing between the n-well and the grounded p-type substrate, if the voltage on the cathode (n-well) is larger than the n-well p substrate junction breakdown voltage. Similarly, if a diode-connected nMOS in the grounded p-substrate is used, charges from the anode or cathode (source or drain) will leak to ground through the parasitic n^+ p substrate junction for high voltages. In both cases, the maximum output voltage that can be generated by the diode pump using these two devices is limited by the breakdown voltage of the parasitic junctions of the CMOS process used.

It is known in the literature that the use of a triple well technology increases the risk of latch-up [39]. As an example, for that reason in the charge pump implementation in [38] a pMOS transistor is used instead of a floating nMOS transistor.

Some processes offer high voltage options, and the main disadvantage of using high voltage devices is their high threshold voltage which implies using a larger gate area and therefore higher parasitic capacitances comparing to using low voltage devices (it is clear from the basic charge pump formulas presented that higher parasitic capacitances and higher threshold voltages degrade pump performance). However, even though a risk of latch-up exists, a charge pump generating negative voltages can be implemented using a triple-well process [42]-[44].

A solution for a charge pump implementation offering several advantages over the implementation with a junction diode or a diode connected transistor is a pump using polysilicon diodes. Examples of pumps using polysilicon diodes are presented in [27], [45]. A cross-section of a polysilicon diode is shown in Fig. 64 and their construction has been discussed when dealing with high resistances on-chip

implementation.

The anode and the cathode of the polysilicon diodes are fully isolated from the silicon substrate, and the voltages on the anode or the cathode of the polysilicon diodes are not limited by the breakdown voltage of the undesired parasitic p-n junction. Using polysilicon diodes, both positive and negative voltages can be generated without danger of the leakage current and latch-up.

Further more, it is shown in [45] that a pump with polysilicon diodes have a higher power efficiency than the other types of diode pump. Using polysilicon diodes hasn't shown to have penalties such as larger area consumption and using polysilicon diodes does not require additional processing steps. As for the amplifier designed in this work, a negative charge pump is needed, polysilicon diode pumps have been chosen. A schematics of the negative charge pump using diodes is shown in Fig. 71.

As mentioned, negative charge pumps implemented in a triple-well technology can be found in the literature. A cross section of a nMOS transistor in a deep nwell in our technology with parasitic bipolar transistor is similar to a cross section of a well diode shown in Fig. 66. It looks as if a negative pump can be implemented in our technology using these devices similarly to examples in the literature, however, to compare the advantages and disadvantages of using nMOS transistors inside a deep n-well and polysilicon diodes a more detailed study is needed and can be done as a continuation of this project. In the analysis of this circuit the influence of all the parasitic bipolar transistors needs to be considered and a proper connection for the deep n-well chosen or a method to avoid parasitic action implemented. If the deep nwell is connected to ground (to turn off the diode between the deep nwell and p-substrate), the minim negative voltage generated by the nMOS pump would be determined by the leakage current that can be tolerated between the pwell and the deep nwell.

As for our particular implementation, for biasing the two microphones, the positive and negative charge pumps need to have the same performance and only opposite sign, matching of the two pumps, positive and negative, when using polysilicon diodes and floating nMOS transistors could be compared as well. At first glance, for our purpose, as we don't need a voltage larger than 10V and have no need for the output current drive, an advanced charge pump implementation using transistors wouldn't be advantageous. However, a fast pump settling time, a well defined pump output voltage and good matching of the two charge pumps is required.

9.7.1 Charge Pump Simulation Results

The positive and negative charge pumps are implemented using N=8, eight stages of polysilicon diodes with width W=1μm and length L=0.5μm (diode characteristics is shown in Fig. 65) and with capacitors C=1pF as shown in Fig. 69 and Fig. 71. This diode size has been chosen as the measurement results, not shown here, have chosen that it has the most conventional diode characteristics among the currently available diodes, the best current drive and is best modeled.

As it will be seen, the chosen size of the capacitor C is much larger than the stray capacitance et each node and MIM capacitors occupying minimal area are chosen. They can resist absolute voltages of at least 11V. Size of the load capacitance C_L is 12pF. A circuit that can be used for providing the two non-overlapping clock signals in anti-phase can be found in any textbook. The amplitude of the

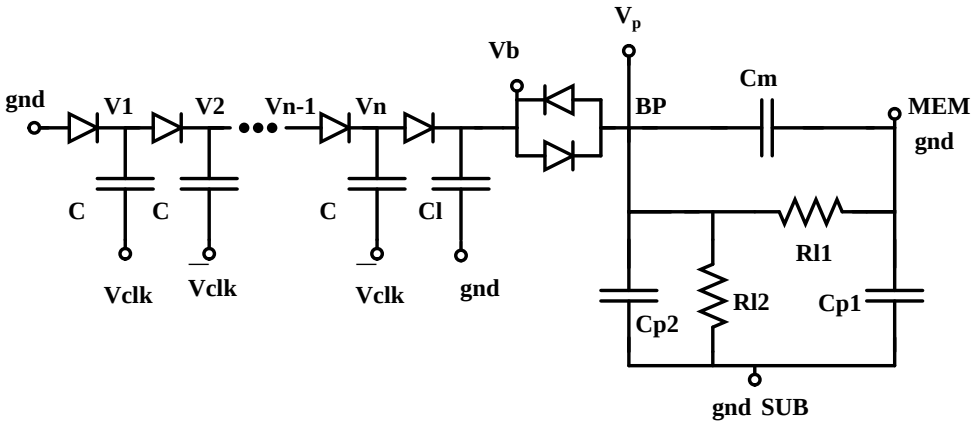


Figure 72: Positive charge pump and the microphone model used in simulations isolated from the pump by back-to-back polysilicon diodes.

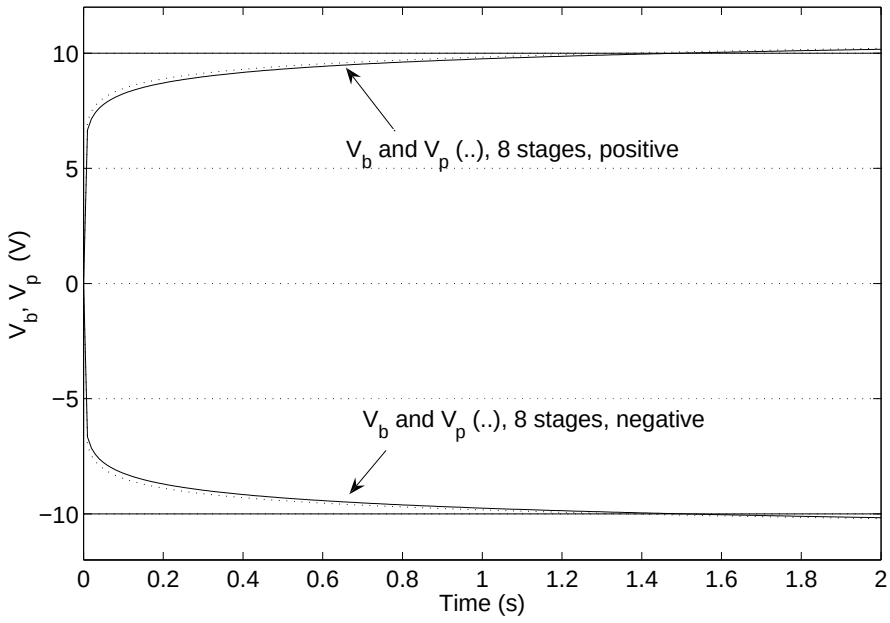


Figure 73: 8-stages positive and negative charge pump simulation results.

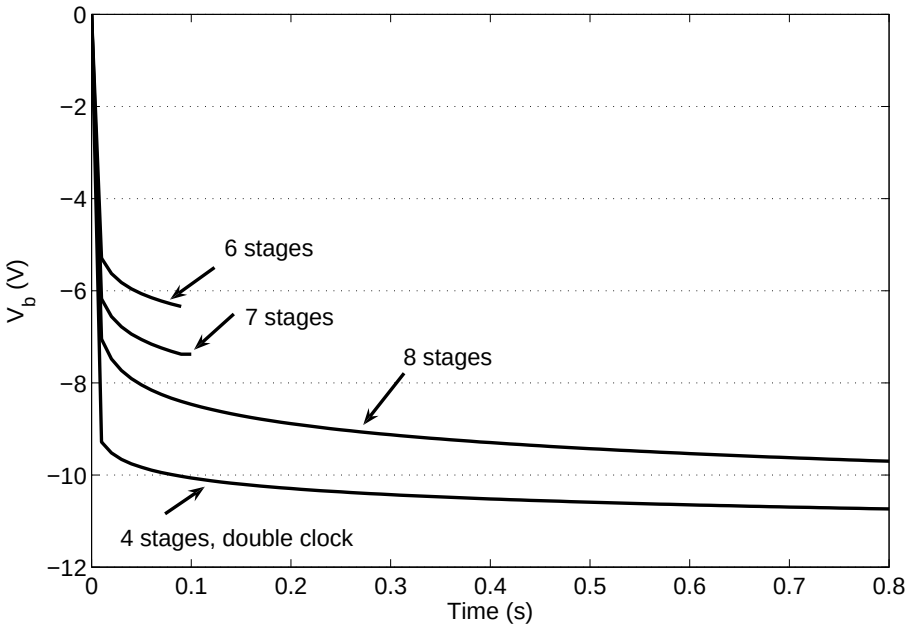


Figure 74: 8-stages negative charge pump simulation results with different number of stages.

clock signal in simulations is 1.45V, the clock frequency used is 2.5MHz and the pump input terminal V_{in} is connected to ground in both positive and negative charge pump.

Simulation are done with the microphone model and with two back-to-back polysilicon diodes with W=1μm and L=0.5μm between the output node of the pump V_b and the microphone back plate V_p as shown in Fig. 72 for the positive pump only. The microphone membrane (MEM) is connected to ground for both negative and positive charge pump and thus the parasitic capacitor from the membrane to ground is shorted. The amplifier decoupling capacitor C_c from Fig. 49 is connected to the microphone back plate (BP).

In Fig. 73 simulation results of the 8-stages positive and negative charge pump are shown. It can be seen that the outputs of both pumps are symmetric and the pump output voltages V_b reach 90% of their final value (±9V) after 250ms. In the same figure the output of the pump after the back-to-back diodes is shown using the dotted line, after 250ms the difference between these two voltages is below 150mV; meaning that the microphone and the diodes do not load the pump significantly (for 150mV the diodes used present impedances larger than GΩ and their current is rather low).

As already noticed in works dealing with charge pumps [31] the pump output voltage slightly increases with time probably due to large impedances presented by the diodes which increase as a function of time. The leakage current of the MIM capacitors used is insignificant and can not be attributed to this voltage increase. Simulations of the pump loaded with a capacitor only without the microphone model and without the back-to-back diodes show almost equal result as the plot of V_b from Fig. 73.

Simulations using other clock frequencies result in the output voltage increasing as a function of time as well. Increasing the load capacitance increases the ramp-up time as expected. As suggested

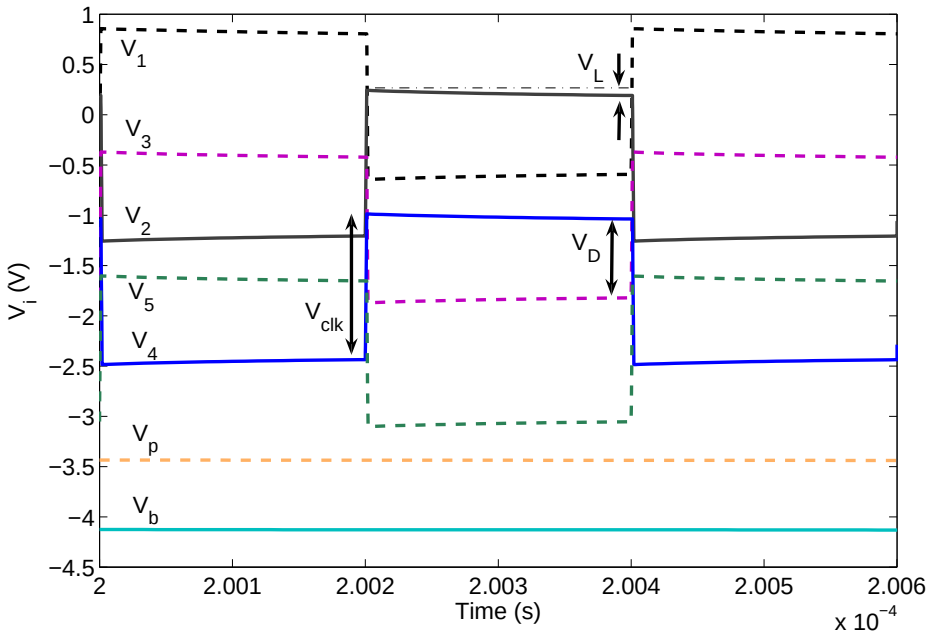


Figure 75: Charge pump simulation results, 8 stages.

in [46] a feedback scheme where a portion of the output voltage from a capacitive divider loading the pump is fed back to regulate the clock amplitude voltage might be investigated in order to design a pump with a time constant output voltage.

In Fig. 74 simulation results of the negative charge pump are shown for several number of stages and grounded input voltage node. Using (174), the diode voltage calculated by reading V_b at 100ms from the curves is $|V_D|$=0.3359V, 0.34537V and 0.3543V for 6, 7 and 8 stages respectively. In the same figure, the output from the pump is shown if a double amplitude clock signal is used with pump with 4 stages only. In this way, the initial start-up time is shorter, but the long time constant for the final value that the pump reaches is not noticeably shorter comparing to the 8-stages case.

In Fig. 75 and Fig. 76 voltages at several nodes of the pump are shown at around $200\mu s$ and around 100ms respectively. Values of the voltage swing at each node $\left(\frac{C}{C+C_s}\right)V_{clk}$, diode voltage V_D and the voltage V_L due to the charging/discharging of the capacitors due to the output current are shown on the figure. As $\left(\frac{C}{C+C_s}\right)V_{clk}$=-1.4489V, it can be calculated that the stray capacitance is very small; simulated diode voltage is -0.784V and V_L is 0.046V. Using (174), calculated output voltage is -4.485V and simulated output voltage is -4.128V. From Fig. 76, after 100ms as the output current diminishes as expected, V_L is very small. A voltage over diodes is smaller than after $200\mu s$, it is equal -0.34982V, and $V_b = -8.467V$. Calculations of V_b give a very close -8.44V. The ripple voltage at the output of the pump is very low, around $1e-5$V.

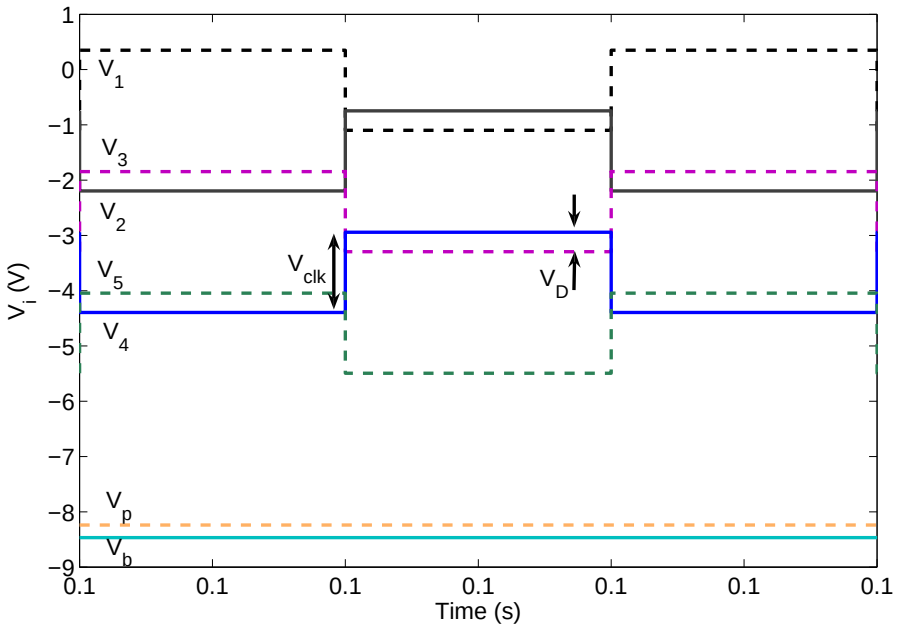


Figure 76: Charge pump simulation results, 8 stages.

10 Conclusion IV

In this chapter a method to increase the sinal-to-noise ratio (SNR) of a MEMS microphone by using two microphone dies has been presented, an idea that Pulse Amsterdam has come up with. Original contribution of this thesis, a novel differential preamplifier capable of handling the signal from to microphones has been described. The noise optimization theory from the previous chapter has been applied to the amplifier designed and the design steps have been explained. The preamplifier designed, implemented in a $0.18\mu m$ CMOS process has been assembled with two microphone dies in a compact small size all silicon chip-scale package (CSP). Measurement results on the chip-scale package have been presented. The results presented show several dB higher SNR comparing to the state-of-the-art MEMS microphones. Using a differential amplifier introduced several advantages comparing to a single amplifier solution as well. Due to the compact packaging technique even though two microphone dies are used, the chip-scale package occupies a very small volume, and is still amongst the smallest microphone components (Table 8). A 3dB improvement in the SNR achieved by this microphone moves MEMS microphones much closer to new applications such as use in hearing instruments. As the improvement has been achieved by designing suitable electronics only, without any redesign of the micromachining parts of the microphone, a significant development cost and the design time have been avoided as well as risks connected with MEMS redesign. Implementation of the basic building blocks used in the design, such as charge pump has been explained also.

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11 Thesis Conclusion and Future Work

11.1 Conclusion

This thesis presents a three-year-and-four-month work on the topic of the design of preamplifiers for condenser microphones. As the thesis is done within a company, the topics described reflect what we believed were interests of the company at that point of time.

The first scientific topic in the chronological order, a task of interest for the employer in the beginning of the study was flicker noise measurements, characterization and modeling. A detailed study of the existing literature has been done, the existing noise theories have been revisited, explained and summarized along with the simulator models. Own measurement set-up has been developed, measurements on own transistors for two CMOS technologies performed, the measurement results explained based on the existing noise theories, noise origin determined and physical noise parameters extracted. The measurement results have been compared with simulations using noise models provided by the foundry and the two technologies compared.

A contribution of this study is that the existing knowledge about the topic has been summarized at one place and a lot of useful information revealed to circuit designers using simulator models without an in depth knowledge. A practical value is that a noise measurement set-up has been developed and characterization done (at DTU), which is not effortless as it is known that the noise measurements are the most arduous measurement task.

A scientific value of this work is the demonstrated understanding of the very complicated flicker noise physics and the ability to use it for the analysis of own data. Each time a new technology node is launched by semiconductor foundries, a measurement results analysis similar to the one we have done here is published. However, even though our experimental data study is alike, the value of our experimental results is not new in the world of science as we don't have the access to the newest technology, that one working for a semiconductor foundry might have. Likewise, we don't have the ability to control the processing steps that the noise depends on for research purpose.

Expecting new contributions concerning the flicker noise theory is very ambitious for a thee-year project about the microphone preamplifier, and is challenging even for a project on noise only and for a research group dealing with transistor modeling. However, we have applied recently derived flicker noise formulas to a problem of noise optimization of a microphone preamplifier. Those formulas are valid for any region of operation and are based on physical noise parameters. They are not a part of any simulator and we have implemented them in own Maple files and used for our preamplifier design. It is difficult for us to evaluate the novelty and the scientific value of that work.

In the introductory part of this thesis, possible methods of sensing a signal from a condenser microphone are explained. Due to a short time left for the design, the analysis is without getting into all the design details of each approach, but shows clearly using which method specifications for a microphone product can be fulfilled at the moment. Although the analysis is simplified and known expressions are used, useful and interesting observations about a preamplifier design are revealed which can not be found elsewhere altogether.

In the final part of this thesis, a design of a preamplifier for two microphones is explained. This

preamplifier is novel and its design is based on the knowledge about a microphone preamplifier design gained in the company. A chip-scale package has been assembled with two microphones and the preamplifier designed, and this work has been presented at the most prestigious conference in the field, which is a first-class achievement of this project especially taking into consideration that during the time assigned for the project, only one chance for making a circuit was possible (after the noise study). Unfortunately, due to a lack of interest and finances no further designs have been submitted resulting in this crown paper only, as both development and research/publishing about IC design are tightly connected with making chips.

11.2 Future Work

This thesis opens a lot of themes that can be investigated as a future work. First of all the topic of the thesis is very attractive, microphones are a relatively new and interesting application of MEMS and a lot of development of MEMS microphones, which can not be used without an interface circuitry, is going on with new products launched on the market.

Some of the non-implemented approaches for interfacing a microphone presented in the introductory part of this thesis can be investigated more deeply and implemented. For example a charge amplifier could be implemented for research purposes both with a MEMS or an ECM microphone. FM modulation principle could be analyzed in more details and maybe implemented with an ECM microphone.

It can be further worked on a preamplifier using a voltage sensing principle in order to improve and analyze its settling time and distortion. PSR ratio for a single transistor amplifier only could be analyzed and improved (without a voltage regulator).

The noise setup developed can be used for measurements of a transistor switching behavior which has been tested only very shortly.

The EKV formulas used for noise optimization match well the measurement results on our preamplifier, however it would be beneficial to verify them on more than one circuit.

Further work on the preamplifier for two microphones could be the development of its second stage, for applications requiring its low output impedance. When making a second stage, DOC techniques used for noise reduction might be implemented as well.

University supervisor Erik had own ideas for the implementation of the preamplifier for two microphones, and can be consulted about them, not to reveal it here. We haven't investigated them in detail due to a lack of time.

Charge pumps have been studied by the company, with several improved variants of them and a lot of measurement data. We have presented an independent short analysis of the circuit for the purpose of completeness of the designed preamplifier for two microphones. As a future work, a study of different charge pump implementations can be done.

As a logical next step, the preamplifier designed can be connected to a $\Sigma - \Delta$ modulator for obtaining a digital output. We believe that it can be easily connected to the modulator used in a company's commercial digital microphone.

A Appendix: Noise Measurements Setup

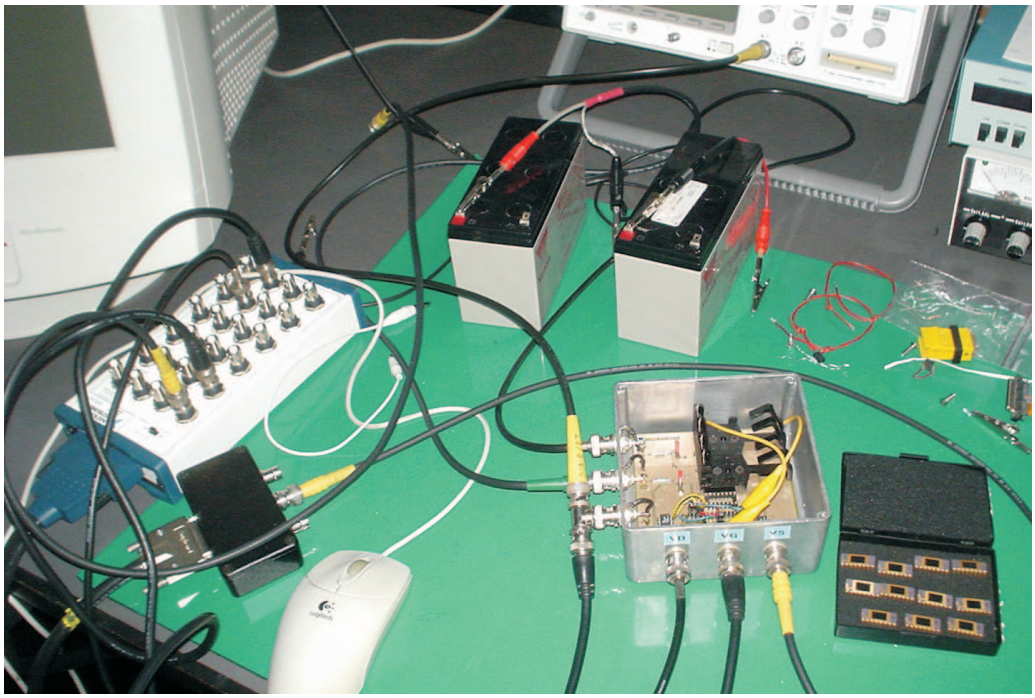

Figure 77: Test setup used for transistor noise characterization.

The test setup used for transistor noise characterization explained in the chapter on flicker noise is shown. The transistor bias voltages are supplied from a PC with an NI card. Batteries are used for biasing the opamps in the setup. Noise spectrum is generated using LabView software controlling the data acquisition card. The oscilloscope is used just for some intermediate checks. The setup is developed and placed at DTU and can be used by students for practical work.

B Appendix: Publications

1) The first article is from NORCHIP conference, 2005. It is about the students Master's thesis work, but was written and presented during the PhD study.
2) The second article is from NORCHIP conference, 2006.
3) The third article is from ISSCC conference, 2009.

A 0.8V, 7μA, Rail-to-Rail Input/Output, Constant G_m Operational Amplifier in Standard Digital 0.18μm CMOS

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Abstract

A two-stage amplifier, operational at 0.8V and drawing 7μA, has been integrated in a standard digital 0.18μm CMOS process. Rail-to-rail operations at the input are enabled by complementary transistor pairs with g_m control. The efficient rail-to-rail output stage is biased in class AB. The measured DC gain of the amplifier is 75dB, and the unity-gain frequency is 870kHz with a 12pF, 100kΩ load. Both input and output stage transistors are biased in weak inversion.

1. Introduction

Constant IC feature size scaling and use of battery powered devices drive nowadays ICs towards reduced supply voltages. Unlike digital circuits, analog circuits do not always benefit from the low supply conditions. The dynamic range is reduced when decreasing signals in a circuit. To increase it, a low-voltage operational amplifier, the main building block in analog and mixed mode circuits, has to deal with signals that extend from rail to rail. An additional challenge in the low-voltage design is the requirement for new circuit solutions because of the fact that the threshold voltage is not scaled proportionally with the supply voltage.

Compact low-voltage power-efficient amplifiers are described in [1-4]. These amplifiers have very good rail-to-rail complementary input stages and current efficient rail-to-rail class-AB output stages. The minimum supply voltage they are able to operate with is equal to two gate-source plus two saturation voltages (2.5 V in [2]).

To ensure operation close to 1V with transistors having relatively high threshold voltages several design techniques such as input level shift [5], bulk driving [6-7], current driven bulk [8], floating-gate MOSFET [9] and DTMOS [10] have been developed. Even though it is possible to overcome the threshold voltage problems, these methods have some disadvantages. Level shifting using resistors increases noise and area, bulk-driven transistors (as well as floating-gate) result in smaller transconductance and therefore less GBW and more noise, are prone to latch-up, and the polarity of the transistor is technology dependent. DTMOS and floating-gate MOSFET require expensive non-standard processing steps.

The amplifier presented here is designed using the approach from [1-2] and a very efficient sub-1V operation is achieved with nMOS (pMOS) transistors having a threshold voltage of 0.45V (-0.5V) by biasing them in subthreshold. In the next chapter the amplifier topology will be presented. Subsequently measurement results will be compared to simulations and finally conclusions will be drawn.

2. Amplifier Description

The amplifier implemented is shown in Figure 1. Its input, output stage and frequency compensation method are described in the following subsections.

2.1. Rail-to-rail Input Stage

A well known method for obtaining a rail-to-rail operation at the input is placing two differential pairs (nMOS and pMOS) in parallel. For low values of common-mode voltage the pMOS transistor pair (M3-M4) will be on, while for high common-mode voltages the nMOS pair (M1-M2) is on. The minimum necessary supply voltage for this configuration is:

$$V_{sup,min} = V_{GSn} + V_{GSp} + V_{DSatn} + V_{DSatp} \quad (1)$$

where V_{GSn} and V_{GSp} are the gate-source voltages of the nMOS and pMOS input transistor pairs, and V_{DSatn} and V_{DSatp} are the saturation voltages of the current sources M9 and M10. For 0.8V operation, the input transistors are biased in weak inversion (2×0.3V + 2×0.1V = 0.8V).

A problem when using a complementary input stage is that the transconductance varies over the input common-mode voltage range, impeding an optimal frequency compensation. In fact, in the middle part of the common-mode voltage range, both input pairs are active at the same time, and the sum of their drain currents is two times the current in the outer part of the common-mode voltage range, when only one of the input pairs is on. Therefore some extra circuitry is needed to keep the total g_m constant. In this amplifier, g_m control is provided by current switches M5-M8. Several g_m control methods have been developed for different regions of operation of input transistors [1, 4]. A good feature of the input stage with the current switches g_m control applied here is that it delivers a constant output current to the summing circuit, consisting of a

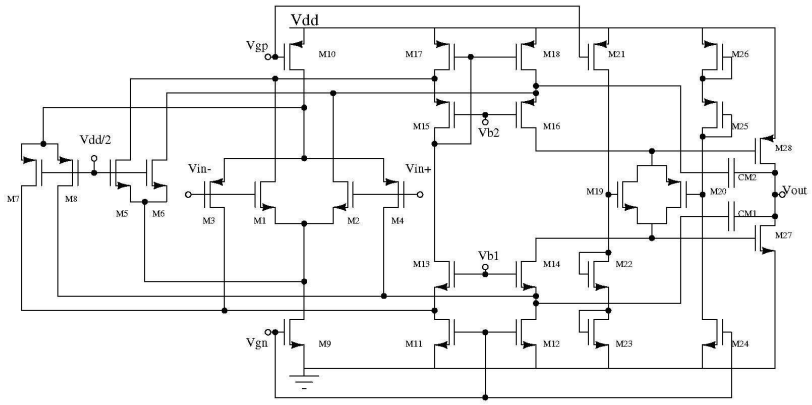

Figure 1: Amplifier Schematics.

high-swing current mirror (M15-M18) and common-gate stages (M13-M14). The summing circuit needs one gate-source voltage (in strong inversion) plus two drain-source voltages for proper operations.

2.2. Class AB Output Stage

To ensure output rail-to-rail operations, the output transistors M27-M28 are connected in a common-source configuration. For the efficient use of the power supply they have to be biased in class AB. Compact class-AB output stages are presented in e.g. [1-3].

In our amplifier, class-AB operations are allowed by the control transistors M19-M20. These transistors are driven by the signal currents from the summing circuit transistors M14 and M16, and their gates are kept at a constant voltage by two pairs of diode-connected transistors (M22-M23 and M25-M26). The diode-connected transistors, the class-AB control transistors, and the output transistor form two translinear loops (M27, M19, M22, M23 and M28, M20, M25, M26), which determine the bias current in the output transistors. Assuming that M22 and M19 have the same gate-source voltages and the same dimensions, M23 and M27 will have the same gate-source voltage as well, and the output quiescent current will be determined by the ratio of the aspect ratios of M27 and M23.

From Fig. 1 it can be concluded that the branch with stacked diodes needs two gate-source voltages plus one saturation voltage for proper operations. In this 0.8V implementation all transistors in the output stage except the current sources are biased in weak inversion. A weak point of this implementation is that the output current varies as a function of the supply voltage.

2.3. Complete Realization

The dimensions of the components shown in Fig. 1 are given in Table 1.

The amplifier is frequency compensated by the cascoded Miller frequency compensation method [2], which, compared to the classical Miller compensation, shifts the non-dominant pole to higher frequencies. This is due to the fact that the cascode transistors are included in the Miller loop, since the compensating capacitors are placed between the drains of the output transistors and the sources of the cascode transistors. The frequency of the non-dominant pole when using the classical Miller compensation depends on the load capacitor, the transconductance of the output transistor, and its gate-source capacitance approximately as $g_m/(C_L + C_{gs})$, and it can be adjusted by changing the current in the output transistor. But since the main goal in this design was a very low current consumption, having at the same time transistors forming translinear loops with two diodes stacked on only 0.7V, it was not possible to obtain optimal frequency compensation with the classical Miller technique, and the cascoded Miller is used instead.

In this implementation, the class-AB control transistors are biased by the summing circuit, which is feasible since the output current of the first stage for the used g_m control method is not dependent of the common-mode voltage. To obtain an output circuit independent of the g_m control method, with minimized noise and minimized depen-

MOST	W(μm)/L(μm)	I_D(I_{REF}=1.09μA)
M1, M2, M5, M6	50/0.36	$I_{REF}/4$
M3, M4, M7, M8	165/0.36	$I_{REF}/4$
M13, M14	10/0.36	$I_{REF}/2$
M15, M16	33/0.36	$I_{REF}/2$
M9, M11, M12	10/6	I_{REF}
M10, M17, M18	33/6	I_{REF}
M24	2.5/6	$I_{REF}/4$
M21	8.25/6	$I_{REF}/4$
M19, M22	30/0.18	$I_{REF}/4$
M20, M25	99/0.18	$I_{REF}/4$
M23	5/0.18	$I_{REF}/4$
M26	16.5/0.18	$I_{REF}/4$
M27	60/0.18	$3I_{REF}$
M28	198/0.18	$3I_{REF}$
CM1, CM2	1.075pF	

Table 1: Transistor dimensions, drain currents (with a common-mode voltage of $V_{DD}/2$), and capacitor values.

dence of the quiescent output current on the supply voltage, the compact operational amplifiers described in [1-2] have two high-swing current mirrors biased by a floating current source. For proper operation the two current mirrors need two gate-source voltages in strong inversion, and this implementation is not feasible for 0.8V operations in the technology used here.

3. Amplifier Performance

The amplifier has been fabricated in a standard digital 0.18μm n-well CMOS process (threshold voltages of 0.45V and -0.5V for nMOs and pMOS, respectively). The chip photograph is shown in Fig. 2.

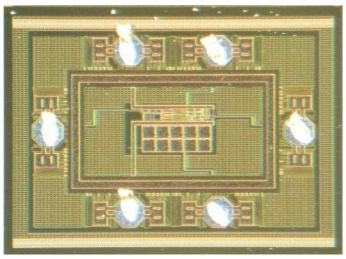

Figure 2: Chip photo.

Using a 1pF Miller capacitor, the simulated unity-gain frequency (GBW) is 1.1MHz for a 5pF load, with a phase margin of 71°. The simulated DC gain is 84dB, while the measured value is 74dB. The capacitive load in the measurement setup is estimated at 12pF in parallel to 100kΩ. The measured unity-gain frequency is 870kHz. When reducing the supply voltage to 0.7V, the amplifier will still be operational, with a GBW reduced to 760kHz. Simulated and measured frequency characteristics are compared in Fig. 3 (V_{DD}=0.8 V, input common-mode voltage V_{COM}=0.4 V).

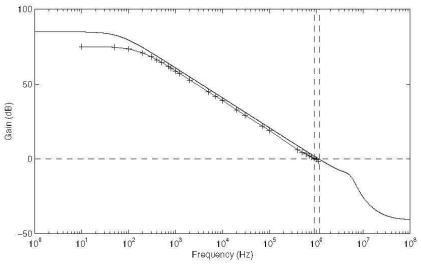

Figure 3: Comparison of the simulated and measured (+) frequency response of the amplifier.

The measured current consumption for this amplifier is 7μA with 0.8V supply voltage, and it is simulated that the supply current will increase to 10.5 μA for V_{DD} of 1.5 V. This increase is due to the increase of the quiescent current in the output transistors for higher supply voltage.

The simulated GBW variation as a function of the common-mode voltage is compared to the measured variation in Fig. 4. The measured variation is 8%, which is very close to the variations for transistors in weak inversion found in the literature [1, 5].

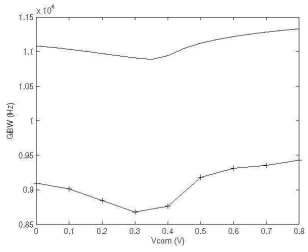

Figure 4: Simulated versus measured (+) variation of the GBW as a function of the input common-mode voltage.

Measurement results when the amplifier is connected in a unity-gain buffer configuration are shown in Fig. 5. Large (300mV) and small (50mV) 250kHz input step signals are shown, along with the respective measured and simulated outputs. The measured slew rate is 0.6V/μs,

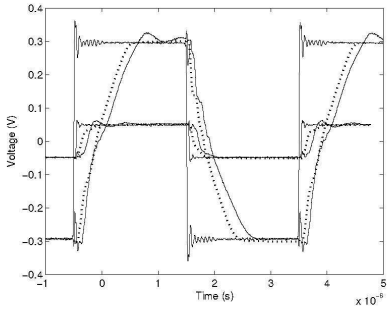

Figure 5: Measured input and output and simulated output (·) signal for unity-gain buffer configuration.

matching well the simulated 0.66V/μs. Due to the high load capacitance, the phase margin of the amplifier is reduced, compared to the simulated value, and therefore an overshoot can be noticed in the measured response. It has been simulated that the frequency response of the buffer starts deteriorating for common-mode voltages 50mV from the supply rails. When the amplifier is loaded resistively in the unity-gain buffer configuration, it has been measured that the output signal will be clipped ±20mV from the supply with a 1kΩ load, while simulations show clipping at V_{DD}-16mV and V_{SS}+10 mV. The simulated value of the maximum current that can be delivered is 2mA for an output voltage 100mV from the supply rails.

Method	Ref.	Tech.	VDD (V)	Gain (dB)	GBW, PM	Load	Isup (μA)	$\frac{GBW}{P}$ ($\frac{MHz}{mW}$)
Compl. pair	[2]	1 μ	2.5-6	85	2.6 MHz, 66 $^\circ$	10 pF, 10 kΩ	180	5.77
Compl. pair	[2]	1 μ	2.5-6	87	6.4 MHz, 53 $^\circ$	10 pF, 10 kΩ	180	14
Compl. pair	[3]	1.6 μ	1.8-7	86	4 MHz, 67 $^\circ$	5 pF, 10 kΩ	230	9.66
Compl. pair	[4]	0.7 μ	1.3-1.8	84	1.3 MHz, 64 $^\circ$	15 pF	350	2.85
Compl. pair level shift	[5]	0.8 μ	1	75	1.8 MHz, 57 $^\circ$	15 pF,1 MΩ	136	13.25
Bulk-driven	[6]	2 μ	1	48	1.3 MHz, 57 $^\circ$	22 pF	300	4.3
Bulk-driven	[7]	0.35 μ	1	70	190 kHz, 60 $^\circ$	7 pF	5	38
Current-driven bulk	[8]	0.5 μ	0.7-1	62	2 MHz, 57 $^\circ$	20 pF	40	71
Floating-gate	[9]	0.35 μ	1.2	65	230 kHz, 62 $^\circ$	9 pF	4.3	44
DTMOS (Simul. only)	[10]	0.18 μ	1	64	35.7 MHz, 64 $^\circ$	5 pF, 10 kΩ	522	68
Compl. pair	This work	0.18 μ	0.8	74	870 kHz, 66 $^\circ$	12 pF, 100 kΩ	7	155

Table 2: Properties of low-voltage amplifiers from literature.

The corner frequency of the flicker noise lies at 2.5kHz, and the thermal noise level is $120\frac{nV}{\sqrt{Hz}}$. The amplifier occupies an area of 0.033 mm^2.

4. Conclusion

The designed amplifier shows very good performances concerning low-voltage, low-power, rail-to-rail operations, and it is capable of driving resistive loads efficiently as well. Its design is based on a robust approach, and low-power operations are achieved by the use of very low bias currents in a modern technology.

The main properties of rail-to-rail, low-voltage amplifiers found in the literature are summarized in Table 2, and the properties of the amplifier designed in this work are listed in Table 3. If the ratio of GBW to power consumption (for the same load) is taken as a figure of merit, as proposed in [2], the amplifier described here shows superior performance compared to the amplifiers in Table 2.

Parameter	Value	Unit
Die area	245×135 (0.033)	μm^2 (mm^2)
Supply voltage	0.8 to 2	V
Supply current	7	μA
Max. out curr. (Sup $\pm$100 mV) *	2	mA
g_m variation	8	%
CMIR*	0.05 to V_{DD}-0.05	V
Out. swing (with 1 kΩ load)	0.02 to V_{DD}-0.02	V
Offset voltage	3.6	mV
Input noise floor	120	$\frac{nV}{\sqrt{Hz}}$
Corner frequency	2.5	kHz
CMRR*	75	dB
Open-loop gain	74	dB
Unity-gain frequency	870	kHz
Unity-gain phase-margin	66	$^\circ$
Slew-rate	0.6	V/μs
PSRR*	56	dB
$\frac{GBW}{P}$	155	$\frac{MHz}{mW}$

V_{DD}=0.8 V, C_L=12 pF, 100 kΩ, T=27 °C
* simulated value, C_L=5 pF

Table 3: Amplifier properties.

5. Acknowledgments

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1/f Noise Characterization in CMOS Transistors in 0.13μm Technology

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Abstract

Low-frequency noise has been studied on a set of n- and p-channel CMOS transistors fabricated in a 0.13μm technology. Noise measurements have been performed on transistors with different gate lengths operating under wide bias conditions, ranging from weak to strong inversion. Noise origin has been identified for both type of devices, and the oxide trap density N_t, the Hooge parameter α_H and the Coulomb scattering parameter α_s have been extracted. The experimental results are compared with simulations using the BSIM3v3 MOS model.

1. Introduction

There is an increasing need for accurate low-noise circuits, as the technology-driven decrease in power supply voltage makes it increasingly difficult maintaining a high signal-to-noise ratio in modern analog designs. It is well known that a reduction in device size leads to an increased 1/f noise. In addition, as low-frequency noise is strongly technology dependent, novel processing steps introduced with technology downscaling lead to performance deviations which are difficult to predict [1]. To achieve an accurate prediction of the impact of 1/f noise on circuit performance, accurate noise modelling is required. Despite more than thirty years of research, a controversy still exists about the physical origin of 1/f noise in MOS transistors. Some authors attribute its origin to fluctuations in the total number of charge carriers [2], some to fluctuations in the mobility of carriers [3], and some to both [4]-[5]. The widely used BSIM3v3 MOS noise model implemented in commercially available circuit simulators is based on the latter approach [6].

In order to investigate the validity of noise models available to a circuit designer, in this work, a low frequency noise analysis is performed on n-channel and p-channel transistors biased both in weak and strong inversion, and both in linear and saturation regime. The noise measurement data are analyzed to identify the noise origin. The physical parameters N_t (oxide trap density), α_H (Hooge parameter), and α_s (Coulomb scattering parameter) have been extracted, and finally measurement data have been compared to simulations using BSIM3v3 noise model with noise parameters provided by the foundry.

2. Noise Models

Two main theories are used to describe the origin of 1/f noise in MOS transistors.

McWhorter carrier number fluctuations (ΔN) theory explains the noise origin by the fluctuations of the channel free carriers due to the random trapping and detrapping of charges in the oxide traps near the Si-SiO_2 interface. Theoretical formulation for the drain current power spectral density S_{I_D}, based on the ΔN theory proposed by Reimbold [7] and Van der Ziel [8] for transistors working in weak inversion, is given by

$$S_{I_D} = \frac{q^4 N_t}{kTWL\gamma C_{ox}^2 \eta^2} \frac{I_D^2}{f} \tag{1}$$

where N_t is the trap density, γ (10^8/cm) is the tunnelling constant for the traps, and η is the weak inversion slope factor, given by (C_{ox}+C_D+C_{it})/C_{ox}, with C_{ox}, C_D and C_{it} being the oxide, depletion and interface trap capacitances per unit area, respectively (W, L, q, kT have their usual meaning). Experimental results in general show that the formalism (1) explains very well 1/f noise in weak inversion. In fact, the value of N_t can be extracted from noise measurements against drain current, if other parameters from (1) are known. Furthermore, this parameter is related to the BSIM noise parameter NOIA as N_t=NOIA/q. For transistors working in strong inversion in the ohmic range, the ΔN-based model of S_{I_D} can be expressed by [9]

$$S_{I_D} = \frac{q^2 kTN_t \mu_{eff}^2}{\gamma} \frac{W}{L^3} \frac{V_{DS}^2}{f} \tag{2}$$

with V_{DS} being drain-source voltage and μ_{eff} effective mobility.

The second 1/f noise theory, Hooge mobility fluctuation ($\Delta\mu$) theory [3], explains the origin of 1/f noise by the fluctuations of bulk mobility with the empirical relation for homogeneous semiconductors, given by

$$S_{I_D} = \frac{\alpha_H}{N} \frac{I_D^2}{f} \tag{3}$$

where α_H is Hooge parameter, constant for a given technology and N the total number of carriers under the gate. After estimation of N, it can be shown [9] that for a MOS transistor working in the linear region the following applies

$$S_{I_D} = \alpha_H q \mu_{eff}^2 \frac{W}{L^3} (V_{GS} - V_{th}) \frac{V_{DS}^2}{f} \tag{4}$$

The measured 1/f noise in n-MOS transistors in strong inversion in the ohmic region usually shows constant S_{I_D}/μ_{eff}^2 versus gate bias voltage, in agreement with (2), which can not be predicted by the $\Delta\mu$ model, because of the bias-independent α_H; thus, the 1/f noise origin for n-devices is attributed to the number fluctuation theory. On the other hand, the observed dependence on the gate bias for the same region for p-channel transistors is following the $\Delta\mu$ theory, in line with equation (4), and can not be explained by ΔN. However, quadratic variation of S_{I_D} versus drain current, following the ΔN model described by (1), is observed for both n- and p-transistors in weak inversion, and can not be explained by the Hooge model. This controversy, known from the experiments published in the literature, has been observed in our experiments as well, which will be presented in the next section.

Recent modelling efforts combine the two previously described approaches in the correlated number and mobility fluctuations ΔN-$\Delta\mu$ model [4]-[5], in an attempt to come to a universal model valid for both n- and p-channel transistors in all operation regions. This model takes into account that the oxide/interface traps, apart from modulating the number of carriers, indirectly interact with the carrier mobility through Coulomb scattering. By this approach, the normalized drain current noise spectral density takes the form presented by Ghibaudo [5]

$$\frac{S_{I_D}}{I_d^2} = [1 + \alpha_s \mu_{eff} C_{ox} \frac{I_D}{g_m}]^2 (\frac{g_m}{I_D})^2 S_{Vfb} \qquad (5)$$

where α_s is scattering parameter and S_{Vfb} is the flatband voltage spectral density given by

$$S_{Vfb} = \frac{q^2 kTN_t}{\gamma WLC_{ox}^2} \frac{1}{f} \qquad (6)$$

Since for weak inversion

$$\frac{g_m}{I_D} \approx \frac{q}{kT} \frac{1}{\eta} \qquad (7)$$

and by neglecting the scattering term in (5), it can be noticed that

$$\frac{S_{I_D}}{I_D^2} = (\frac{g_m}{I_D})^2 S_{Vfb} \qquad (8)$$

equals equation (1). Similarly, by plugging in the formulas for μ_{eff} and $\frac{I_D}{g_m}$ in the linear region in (5), it can be shown that the input referred noise voltage density takes the form

$$S_{V_g} = [1 + \alpha_s \mu_0 C_{ox} (V_{GS} - V_{th})]^2 S_{Vfb} \qquad (9)$$

where μ_0 is the low-field mobility and V_{GS} the gate-source voltage.

The ΔN-$\Delta\mu$ model described shows a satisfactory fitting to the experimental data for both p- and n-channel devices. However, critical discussions on its exactness exist [10]. A form of the unified model noise expression (5)-(9) is implemented in the BSIM3v3 circuit simulator model [6].

3. Experimental Study

3.1. Measurement Set-Up

The devices studied are fabricated in a 0.13μm CMOS technology with oxide thickness 2.4nm, n+/p+ poly gate, shallow trench isolation and Co-silicided drain, source and gate. All the transistors tested have width W=10μm and different lengths. Transistors of the same type have common gate, source and bulk connections, and separate drains. Prior to noise measurements, DC characteristics $I_D(V_{GS})$ and $g_m(V_{GS})$ have been measured. From the DC characteristics for V_{DS}=50mV using the function $\frac{I_D}{\sqrt{g_m}}$ as described in [11], the conduction parameters μ_0, V_{th}, ΔL and S (S=$(\frac{dlogI_D}{dV_{GS}})^{-1} = 2.3\frac{kT\eta}{q}$), given in Table 1, have been extracted for both p- and n-transistors. The drain current noise of the tested devices has been amplified by a low-noise amplifier AD707JN connected in a transconductance configuration, and measured for different transistor bias voltages. The amplifier has been biased using batteries, while the variable voltage values supplied to the DUT have been generated from a PC using the NI6289 high precision data acquisition card. The same card has been used for measurements with the noise spectra obtained with help of NI software. Lorentzian-like spectra usually observed on the top of 1/f noise for small area or minimum size devices have not been taken into account. The same noise behavior has been observed on three measured samples.

L (μm)	0.13	0.26	0.5	1	2
$V_{thn}(V)$	0.41	0.395	0.372	0.360	0.336
$V_{thp}(V)$	0.365	0.364	0.353	0.349	
S_n (mV/dec)	86.23	84.97	84.19	95.7	97.05
S_p(mV/dec)	96.32	87.62	91.66	92.6	
ΔL_n (μm)			0.01		
ΔL_p (μm)			0.015		
μ_{0n} (cm^2/Vs)			221		
μ_{0p} (cm^2/Vs)			60		

Table 1: Extracted Transistor Conduction Parameters (W=10μm) for n- and p-MOS.

3.2. Results Discussion

The plots of the normalized drain current power spectral density S_{I_D}/I_D^2, and the corresponding $(g_m/I_D)^2$ ratio versus drain current are shown in Fig. 1 and Fig. 2 for n- and p-transistors respectively, working in the ohmic region. Analysis of these plots is considered a generic procedure to distinguish between the 1/f noise mechanisms. As explained by equations (5)-(8), if there is a good correlation of the normalized drain current noise with the corresponding transconductance to drain current ratio squared, the ΔN model dominates, which is clearly the case for our n-transistors. On the other hand, for p-transistors in Fig. 2, a departure from the $(g_m/I_D)^2$ characteristics in strong inversion can be explained by the influence of additional correlated mobility fluctuation. From the S_{I_D}/I_D^2 weak inversion plateau, using the equation (1) and the slope factor value from Table 1, the N_t values are calculated. For both types of devices, the value of N_t is about $3.5 \cdot 10^{17} - 4.5 \cdot 10^{17} (eV^{-1}cm^{-3})$. The value of N_t for n-transistors in strong inversion matches the one for weak inversion.

The input-referred noise power spectral density is plotted in Fig. 3 as a function of the effective gate-source volt-

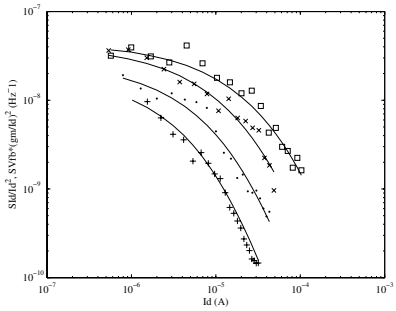

Figure 1: Normalized drain current noise S_{I_d}/I_D^2 and $(g_m/I_D)^2$ ratio of(-) versus drain current for V_{DS}=50mV for NMOS with various transistor lengths. L=0.26(□), 0.5 (×), 1 (•) and 2 (+) μm.

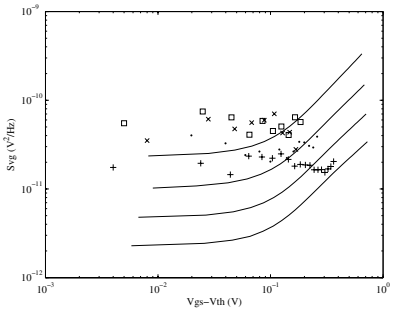

Figure 3: Input referred noise S_{V_g} versus gate overdrive voltage for V_{DS}=50mV for various NMOS transistor lengths. Simulation (-), L=0.26(□), 0.5 (×), 1 (•) and 2 (+) μm.

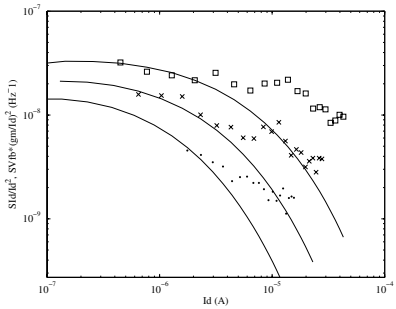

Figure 2: Normalized drain current S_{I_d}/I_D^2 noise and $(g_m/I_D)^2$ ratio (-) versus drain current for V_{DS}=50mV for various PMOS transistor lengths. L=0.26(□), 0.5 (×) and 1 (•) μm.

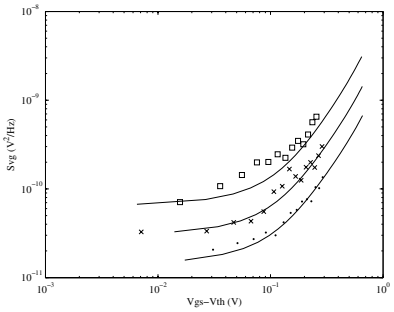

Figure 4: Input referred noise S_{V_g} versus gate overdrive voltage for V_{DS}=50mV for various PMOS transistor lengths. Simulation (-), L=0.26(□), 0.5 (×) and 1 (•) (+) μm.

age for n-transistors, and in Fig. 4 for p-transistors (V_{DS} is 50mV). From these figures, the noise origin observed in Fig. 1 and 2 can be confirmed by the fact that the input noise does not depend on V_{GS} for n-channel transistors, while it is proportional to V_{GS}-V_{th} for p-channel transistors as predicted by (2) and (4), respectively. In our experiments, the same origin has been confirmed by the plot of S_{I_D} versus V_{GS}, not shown here. The occasionally observed S_{I_D} dependence on V_{GS} for high overdrive voltages [12], due to the drain and source series resistances can not be observed for the relatively low bias voltages in Fig. 3. The solid lines in Fig. 3 and 4 are the results obtained by BSIM3v3 simulations. It can be seen that the simulator model predicts very well the noise of p-transistors, while discrepancies exist for the n-channel in linear region. The model predicts dependence on the gate bias similar to p-channel bias dependance. This might be due to the fact that for correct modelling when the ΔN model dominates, similarly to α_H, the NOIB parameter should be proportional to $(V_{GS} - V_{th})^{-1}$. Besides that, it can be seen in Fig. 3 that the model provides different value of the flatband voltage, compared to the measured one. The mean value of α_H for p-transistors with different dimensions is about $4.5 \cdot 10^{-4}$. This value is obtained from the measurement data by using a formula similar to (4) with S_{I_D} expressed as a function of I_D, V_{GS} [9] that does not require the measurement of mobility attenuation factor θ. The values of α_s for p-channel transistors, extracted using (9), have values $7.5 \cdot 10^4 - 9.5 \cdot 10^4$ (Vs/C). The values extracted are similar to the the values reported for the same technology node [13].

S_{I_D} versus drain current for V_{DS}=0.45V for various dimensions of p- and n-transistors is shown in Fig. 5 and 6, along with the simulated data. As expected, the drain current spectral density shows a quadratic dependence on the drain current in weak inversion for V_{DS}=450mV as well as for V_{DS}=50mV. As for the transistors working in linear region, measurements for p-channel transistors match very well simulations, while for n-transistors discrepancies are observed. The slope of the curve of S_{I_D} versus

drain current is the same for measured and simulated data in Fig. 5 while the measured values are somehow greater than simulated.

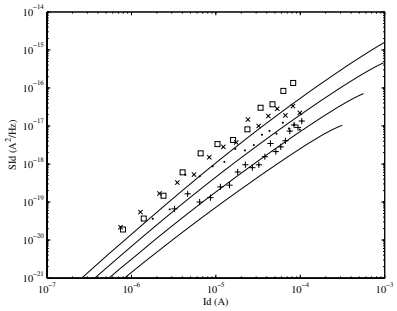

Figure 5: Drain noise spectral density S_{I_D} versus drain current for V_{DS}=450mV for various NMOS transistor lengths. Simulation (-), L=0.26(□), 0.5 (×), 1 (•) and 2 (+) μm.

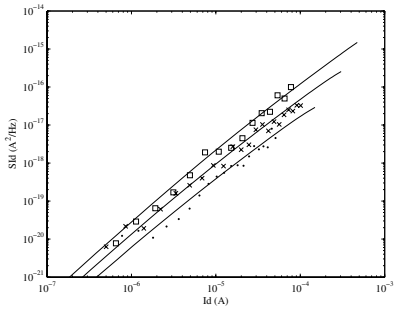

Figure 6: Drain noise spectral density S_{I_D} versus drain current for V_{DS}=450mV for various PMOS transistor lengths. Simulation (-), L=0.26(□), 0.5 (×) and 1 (•) μm.

4. Conclusion

In this work, low frequency noise has been investigated on MOS transistors from 0.13μm technology. It has been observed that the noise in n-transistors originates from the number fluctuation theory, while the noise in p-MOS is due to the number fluctuations with correlated mobility fluctuations. Values of the physical parameters extracted match well the values for similar technologies. The simulation result show very good match with the measured data for p-transistors, while some discrepancies for n-transistors are observed.

5. Acknowledgments

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20.6 A Compact CMOS MEMS Microphone with 66dB SNR

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Silicon MEMS microphones that offer small size, ease of integration with CMOS electronics, and the ability to withstand lead-free solder reflow cycles, are becoming increasingly popular for high-volume consumer electronic products, and are competing in price and performance with traditional electret condenser microphones [1]. The design of a MEMS microphone, consisting of a compliant membrane and a stiff back-plate forming a variable capacitor, is a challenging task with a number of design trade-offs [2]. For cost reasons, a small-area membrane is desired; however, lower acoustical noise is obtained with a larger membrane. In this work, we demonstrate a method to increase the SNR of a microphone system without the need for a complicated and risky MEMS die redesign. An SNR of 66dB is achieved using two microphones (instead of a single one) in a differential configuration, thus doubling the total membrane area.

A MEMS microphone is biased by a high DC voltage V_b generated on-chip from a (low) power supply. The microphone sensitivity S is given by $S = V_b \cdot \Delta C_m/(C_m \cdot \Delta P)$ where C_m is the microphone capacitance, ΔP the sound pressure level (SPL), and ΔC_m the capacitance change in response to ΔP. When two microphones are biased by voltages having opposite polarities (i.e., V_b and $-V_b$) and ΔP is applied, the microphones produce signals of opposite polarities [3]. When these differential signals are fed to a differential amplifier, a 3dB improvement in SNR can be achieved compared to a single-microphone design. It is important to note that a MEMS microphone has limited SNR due to its own intrinsic acoustical noise. The microphone SNR is first-order independent of V_b, and for the die used here its value is between 63dB and 66dB depending on process details. If the amplifier does not deteriorate the SNR, a two-microphone solution can indeed yield a 3dB SNR improvement.

A simplified schematic of the amplifier is shown in Fig. 20.6.1. The DC-blocking capacitors C_c are much larger than C_m. The diode pairs $D_{p1,p2}$ and $D_{p3,p4}$ are necessary to provide high output impedance between the microphone and the charge pump delivering the bias voltage; in order to avoid leakage currents and latch-up hazards due to the bias voltages, polysilicon diodes isolated from the substrate are used. Two more sets of diodes ($D_{1,2}$ and $D_{3,4}$, realized as 6V n^+-p_{well} junctions inside a deep n-well) are necessary to provide a DC path to the gates of the PMOS differential pair, forming the basic gain stage. The zero-current dynamic resistance presented by these diodes is extremely high, so that the poles of the transfer function from microphones to differential output (V_{op} - V_{on}) are well below 20Hz.

The role of the feedback amplifier (FA) is to speed-up the start-up transient. If no FA is used, the different polarities of the bias voltages V_b and $-V_b$ unbalance the voltages at the gates of M_1 and M_2 during start-up, causing the entire bias current to flow through M_2; simulations show that proper functionality would not be recovered even after hundreds of seconds. The FA equalizes the two gate voltages, resulting in a settling time for the differential gain of less than 2s, which is fast enough for any application. This fast settling time is yet another advantage of the differential operation (together with a much higher insensitivity to power-supply-induced noise and electro-magnetic interference). It should be noted that the signal appearing at the output of the FA tends to interfere with the normal operation of the main amplifier, causing distortion. This deleterious behavior is suppressed by diodes $D_{5,6}$, whose task is to limit the feedback signal. The noise generated by all diodes, and primarily by $D_{1,2}$ and $D_{3,4}$, is negligible after less than 3s. Capacitors $C_{5,6}$ enforce the stability of the FA.

The amplifier is implemented in a 0.18µm 3M triple-gate CMOS process. 6V PMOS transistors are chosen for the input pair, as they produce less flicker noise than NMOS transistors. Input-referred noise minimization (including both flicker and white noise) is performed both through calculations (using the EKV MOS equations in the moderate inversion region) and simulations (using the BSIM3v3 MOS model). The optimal $M_{1,2}$ width (W) is determined for several $M_{1,2}$ lengths (L) and bias current I_{bias}, and the overall optimal set of values is W=600µm, L=3µm, I_{bias}=53µA. Noise measurements show that 1/f noise has a slightly higher impact than does white noise, when both contributions are A-weighted. The expected SNR degradation introduced by the amplifier is lower than 1.5dB for V_b=±10V. The amplifier consumes 120µA at 1.8V.

The amplifier differential output voltage for an SPL of 94dB (i.e., 1Pa) and V_b=±10V at 1kHz is 21mV_{rms} with an amplifier gain of 8dB, resulting in a two-microphone sensitivity of 8.4mV_{rms}/Pa. The frequency response under the same conditions is measured with a TBS50 pyramid testbox, with frequency range of 60Hz to 9kHz, and is shown in Fig. 20.6.2. The transfer function is expected to be flat until at least 20kHz. A plot of the THD as a function of the SPL at 1kHz is shown in Fig. 20.6.3. No significant distortion due to the FA is observed, and the THD is below 1% for an SPL below 112dB. Increasing $|V_b|$ increases the microphone sensitivity, resulting in higher microphone output voltages, as shown in Fig. 20.6.4 (top). However, if V_b reaches ~12.2V, the microphone collapses, with the membrane sticking to the bottom plate. Functionality can be restored by discharging the microphone to 0V. The A-weighted 20Hz-to-20kHz rms differential output noise is shown in Fig. 20.6.4 (bottom). At low V_b values, noise almost totally comes from the amplifier (5µV_{rms}), while at higher V_b values the microphone noise becomes dominant. For the nominal condition V_b=10V, the SNR deterioration caused by the amplifier is ~1.0dB. An SNR vs. V_b plot is shown in Fig. 20.6.5, where an SNR of 66.5dB is achieved at V_b=10V (the SNR drops by only ~1dB at a more conservative V_b of 8.5V). The same figure shows that using only one microphone reduces the SNR by 3-4dB, as expected.

Figure 20.6.6 presents a comparison with other MEMS microphone products with data from available data sheets, showing that this work achieves an SNR improvement of several dB. Photographs of CMOS amplifier and MEMS microphones are displayed in Fig. 20.6.7. Contacts between the microphones and amplifier are provided, with negligible parasitic capacitance, through connections on the silicon substrate on which both microphones and amplifier are flip-chip mounted. The amplifier die size is 3.2×0.93mm^2, the membrane diameter of the microphones is 1.05mm, and the volume of the complete chip-scale package (CSP) is 2.6×3.2×0.865mm^3.

This size is chosen to allow the use of a pair of silicon substrate dies already employed in a commercially available digital microphone CSP (with dimensions 2.6×1.6×0.865mm^3, using a single MEMS microphone and a single substrate die) without redesign. Due to compact packaging, the new microphone CSP occupies less area than the products from Figure 20.6.6, despite the use of two MEMS microphones.

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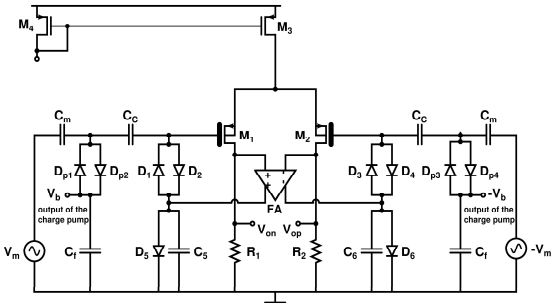

Figure 20.6.1: Circuit schematic of the microphone preamplifier.

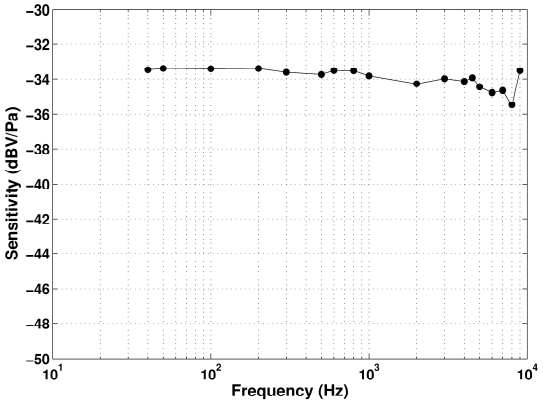

Figure 20.6.2: Frequency response of the system at 94dB SPL.

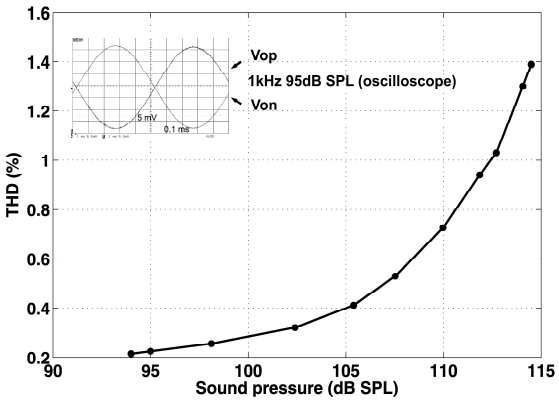

Figure 20.6.3: THD of the differential output voltage vs. SPL @ 1 kHz.

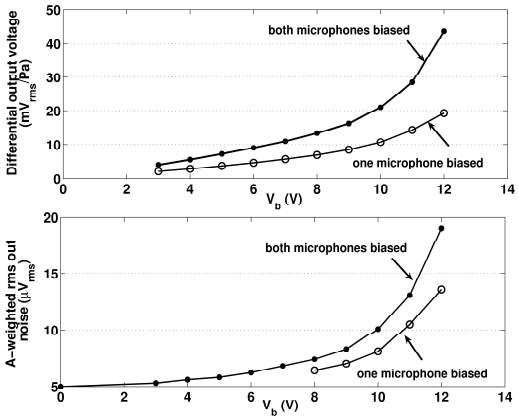

Figure 20.6.4: Top: Differential output voltage vs. microphone bias. Bottom: A-weighted differential output noise vs. microphone bias.

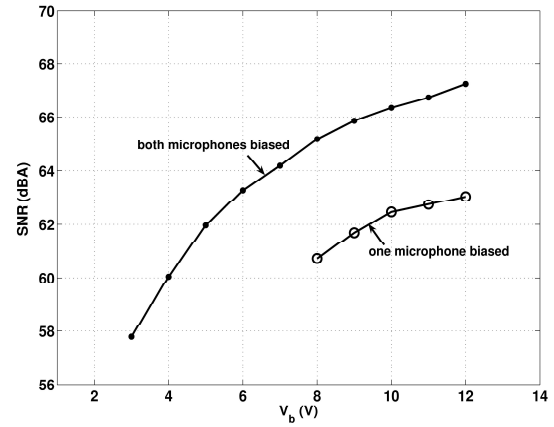

Figure 20.6.5: SNR vs. microphone bias.

	Size, smallest available (mm)	Sensitivity (dBV @1Pa, 1kHz)	SNR (dB@1Pa, A-weighted)	Response (Hz)	V_{cm} (range) (V)	I_{cm} (μA)	PSRR (dB)	THD (% @dB SPL, 1kHz)	R_{cm} (Ω)
this work	**2.6×3.2×0.865**	**-33**	**65.5**	**20-20k**	**1.8 (1.6-3.6)**	**120**	**>55**	**0.4@104**	**8.9k**
[4]	2.53×1.6×0.865	-40	61	20-20k	1.8 (1.64-2.86)	330	>60	2@104	500
[5]	4×4×1.8				(2.8-3.6)				
[6]	4.72×3.76×1.25	-42	59	100-7k	2.1 (1.5-3.3)	80	55	0.1@104	7
[7]	4.72×3.76×1.25	-22 or -42	59	100-10k	(1.5-3.6)	<350 or <250	>40	1@100	<300
[8]	4.72×3.76×1.25	-35 to -30 or -40 to -35 or -45 to -40	57	100-7k	2.1 (1.5-3.6)	120	45	1@104	100
[9]	4.72×3.76×1	-37	62	100-12k	1.8 (1.5-3.6)	200	>50	3@105	200
[10]	4.72×3.76×1.25	-42	57	100-16k	(1.5-3.6)	150			100
[11]	4.3×3.4×1.28	-42	55		(1.5-3.6)				
[12]	3×4×1	-44	55		2	500			

Figure 20.6.6: Performance comparison with commercially available products.

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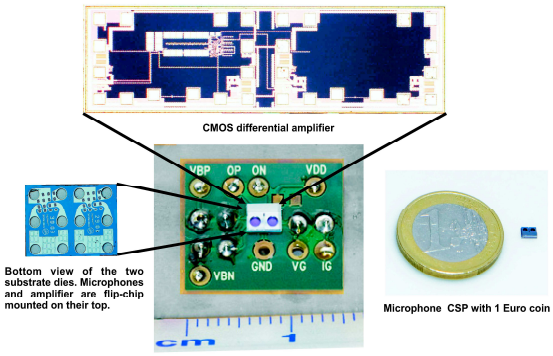

Figure 20.6.7: Photographs of CMOS amplifier, substrate dies, and test PCB with mounted microphone CSP.

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